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# Suzhou2-LA

CPU : Intel Arrandale  
 Chip Set : Intel Ibex Peak(HM55)  
 GFX : PARK/M92 + 512MB VRAM  
 Remarks : Calpella Platform

Model Name : Suzhou2-LA  
 PBA Name : MAIN  
 PCB Code : BA41-01298A  
 Dev. Step : MP  
 Revision : 1.0  
 T.R. Date : 2010.04.01

Design	CHECK	APPROVAL
Zhu Jian	Guo Lei	BC LEE

■ Owner : SEC Mobile R & D Signature : X

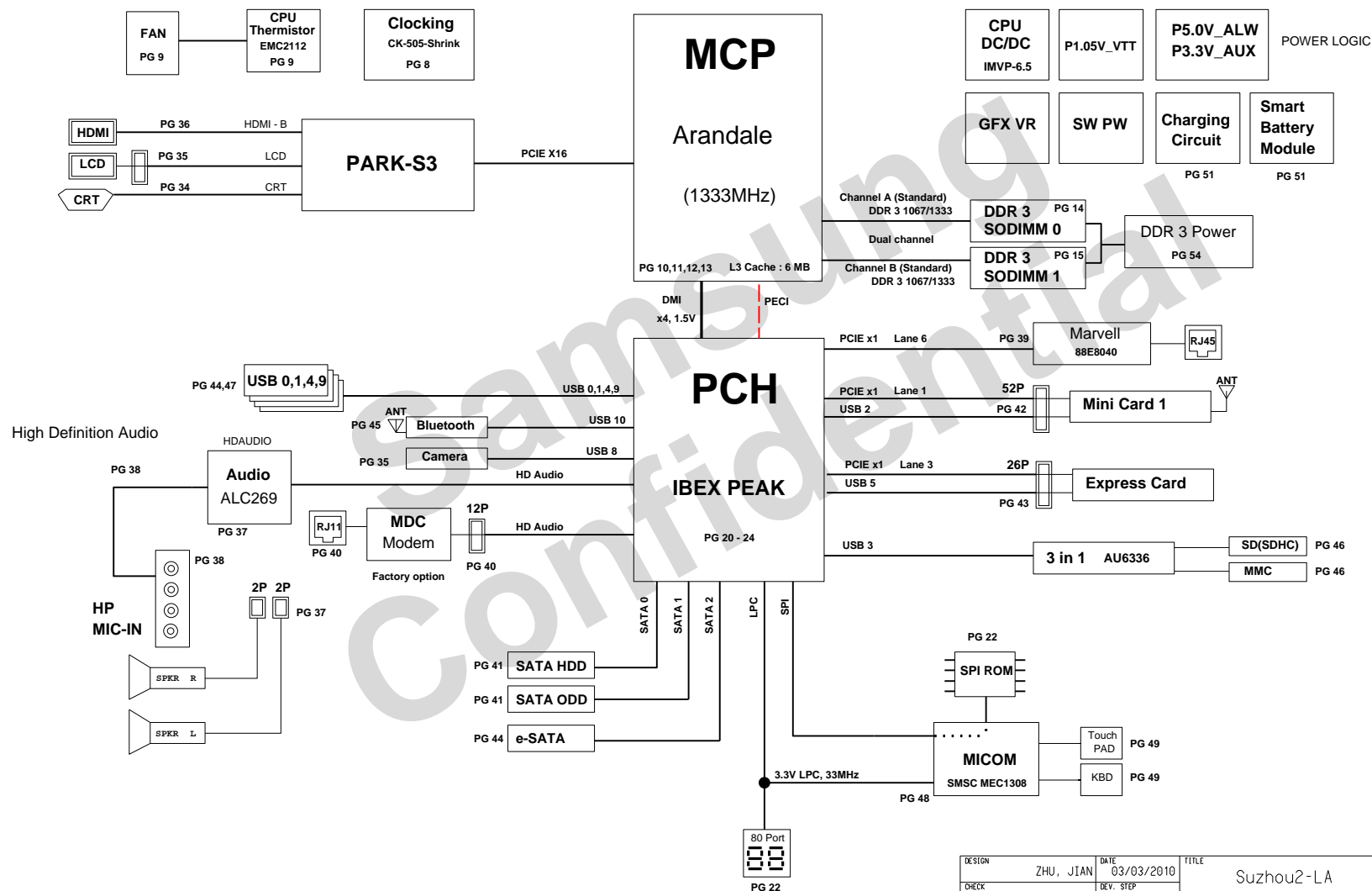
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DESIGN	ZHU, JIAN	DATE	03/03/2010	TITLE	Suzhou2-LA	SAMSUNG ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV	MAIN		
APPROVAL	BC, LEE	REV	1.0	COVER		
MODULE CODE		LAST EDIT	March, 3, 2010 8:43:54 PM	PAGE	1 OF 56	

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**BLOCK DIAGRAM**

DESIGN	ZHU, JIAN	DATE	03/03/2010	TITLE	Suzhou2-LA MAIN BLOCK DIAGRAM	<b>SAMSUNG</b> ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV			PART NO. BA41-XXXXXA
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE		LAST EDIT				

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**BOARD INFORMATION****SCHEMATIC ANNOTATIONS AND BOARD INFORMATION**

Voltage Rails		Active in
VDC P3.3V_MICOM P5.0V_ALW P5.0V_STB	Primary DC system power supply (7 to 21V) 3.3V always power rail (for Micom) 5.0V always power rail 5.0V always power rail	<b>S4 - S5</b>
P5.0V_AUX P3.3V_AUX P1.5V_AUX	5.0V switched on power rail (off in S4-S5) 3.3V switched on power rail (off in S4-S5) 1.5V power rail for DDR (off in S4-S5)	
P5.0V P3.3V P1.8V P1.5V P0.75V	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.8V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 0.9V power rail for DDR (off in S3-S5)	
VCC_CORE EGFX_CORE P1.05V (VCCP) P1.1V_VTT	Core Voltage for CPU Core Voltage for GPU VCC for Clarkfield & IBEX Peak VTT for CLARDSFIELD & IBEX Peak	

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	1	Mini Card 1 (WLAN)
1	SYSTEM PORT 1	2	NC
2	Mini PCI Express 1	3	EXPRESS CARD
3	NC	4	NC
4	SYSTEM PORT 4	5	NC
5	EXPRESS CARD	6	NC
6	NC (N/A WITH HM55)	7	NC (N/A WITH HM55)
7	NC (N/A WITH HM55)	8	NC (N/A WITH HM55)
8	Multi Memory Card Controller		
9	SYSTEM PORT 9		
10	Bluetooth		
11	Camera		
12	NC		
13	NC		

SATA PORT Assign	
PORT #	ASSIGNED TO
0	HDD
1	ODD
2	(N/A WITH HM55)
3	(N/A WITH HM55)
4	e-SATA

**Crystal / Oscillator**

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	IBEX-PEAK	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN
Crystal	25MHz	IBEX PEAK	

**LCD Pannel Detect (TBD)**

Devices	Resolution	PANNEL_DETECT_0

**I<sup>2</sup>C / SMB Address**

Devices	Address	Hex	Bus
IBEX PEAK	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M Shrink(Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
Thermal Sensor on board	1101 100x	98h	
Power thermal management TS	1101 011x	96h	

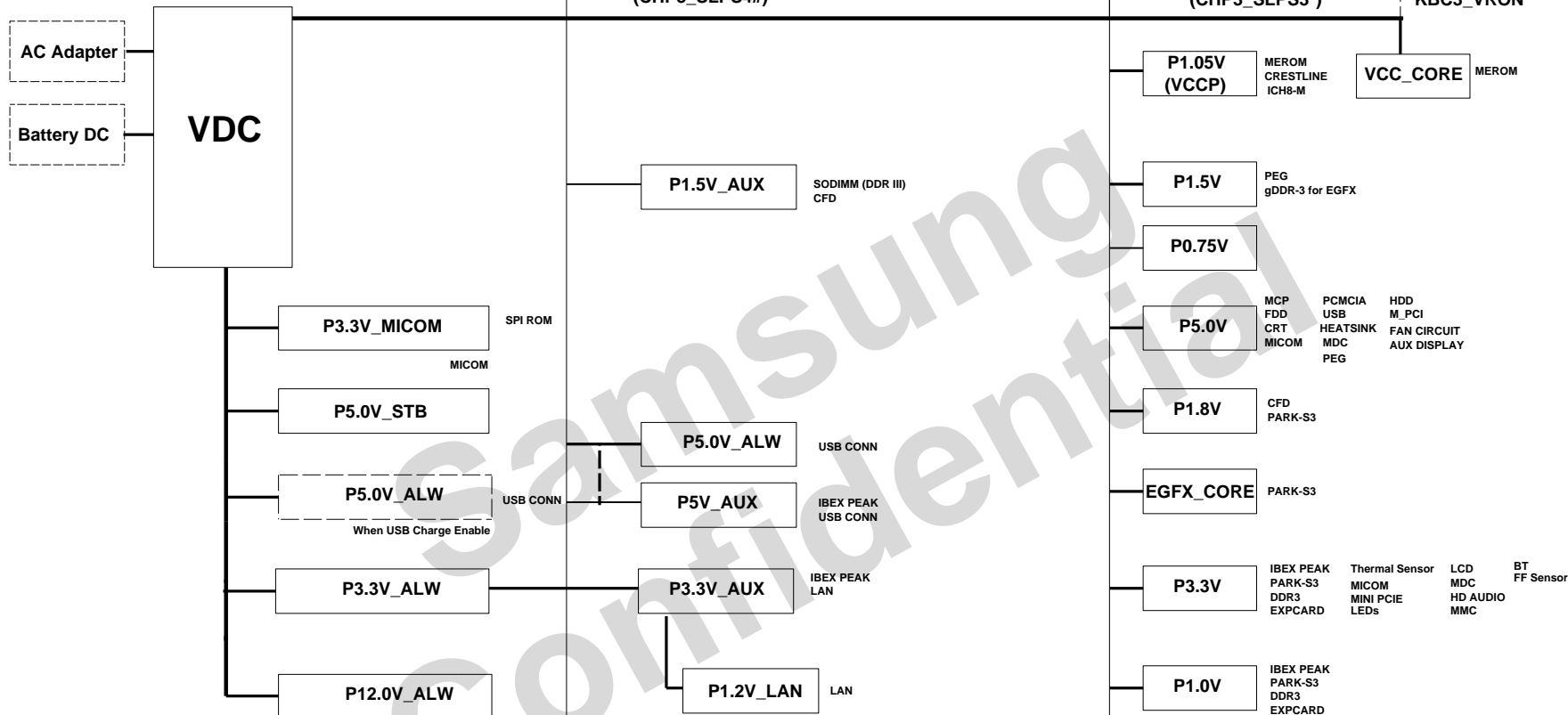
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APPROVAL	BC, LEE	REV	1.0			
MODULE CODE		LAST EDIT	March, 3, 2010 8:44:25 PM	PAGE	3	OF 56

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**POWER DIAGRAM**

Rev 0.1



Power On/Off Table by S-state

Rail \ State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

S5-S4

S3

S0

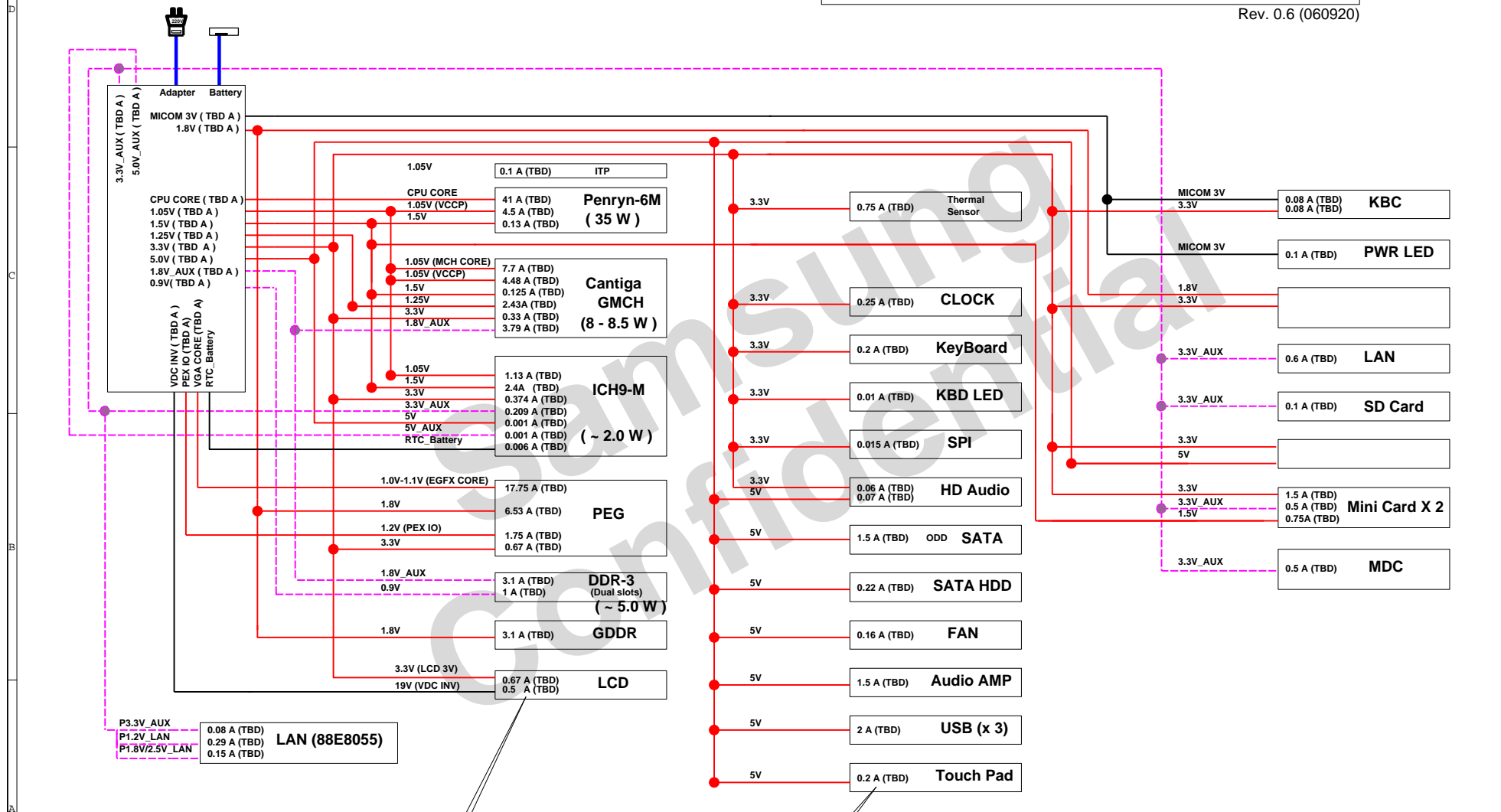
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APPROVAL	BC, LEE	REV	1.0			
MODULE CODE		LAST EDIT				
March, 3, 2010 8:44:41 PM						PAGE 4 OF 56

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**POWER RAILS ANALYSIS**

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

DESIGN	ZHU, JIAN	DATE	8/14/2009	TITLE	Suzhou2-LA MAIN	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01190/
CHECK	GUO, LEI	DEV. STEP	PV	POWER RAILS ANALYSIS		
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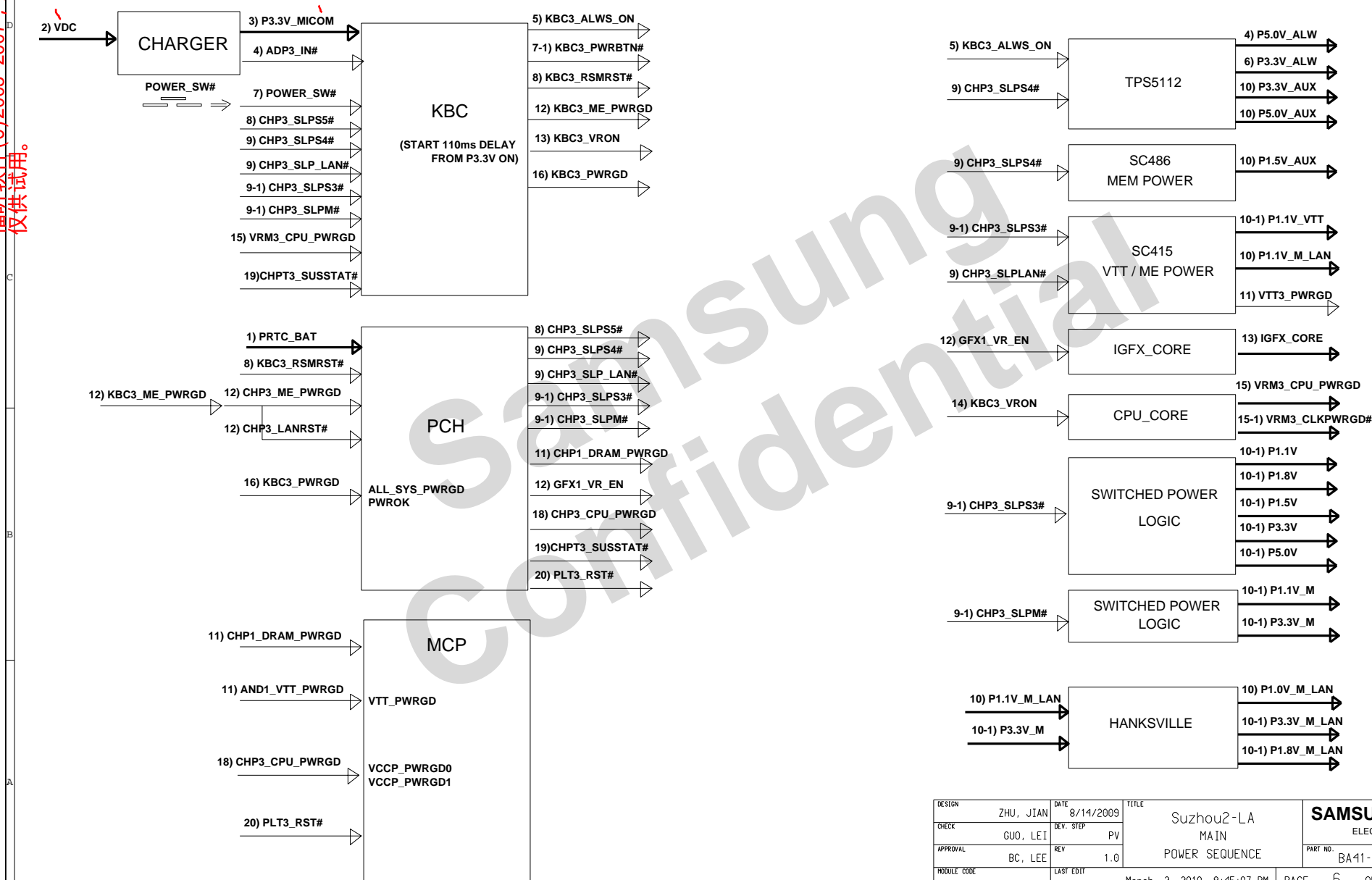
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## PRELIMINARY

## POWER SEQUENCE

Rev. 0.5



DESIGN	ZHU, JIAN	DATE	8/14/2009	TITLE	Suzhou2-LA MAIN POWER SEQUENCE	SAMSUNG ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV			PART NO. BA41-01190/
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE		LAST EDIT	March, 3, 2010 8:45:07 PM	PAGE	6	OF 56

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**CLOCK DISTRIBUTION** Rev. 0.1**Arandale**

BCLK 133M

DMI 100M

DP 120M

XTAL

PLL1

133M, 100M  
HCLK[0:1], SRC\_2

PLL2

96M  
DOT96

PLL3

27M/27M\_SS

PLL4

100M  
SATA / SRC\_1

14.318MHz

PLL  
&  
SSC  
BLOCK

DESIGN	ZHU, JIAN	DATE	8/14/2009	TITLE	Suzhou2-LA MAIN	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01190/
CHECK	GUO, LEI	DEV. STEP	PV			
APPROVAL	BC, LEE	REV	1.0	CLOCK DISTRIBUTION		
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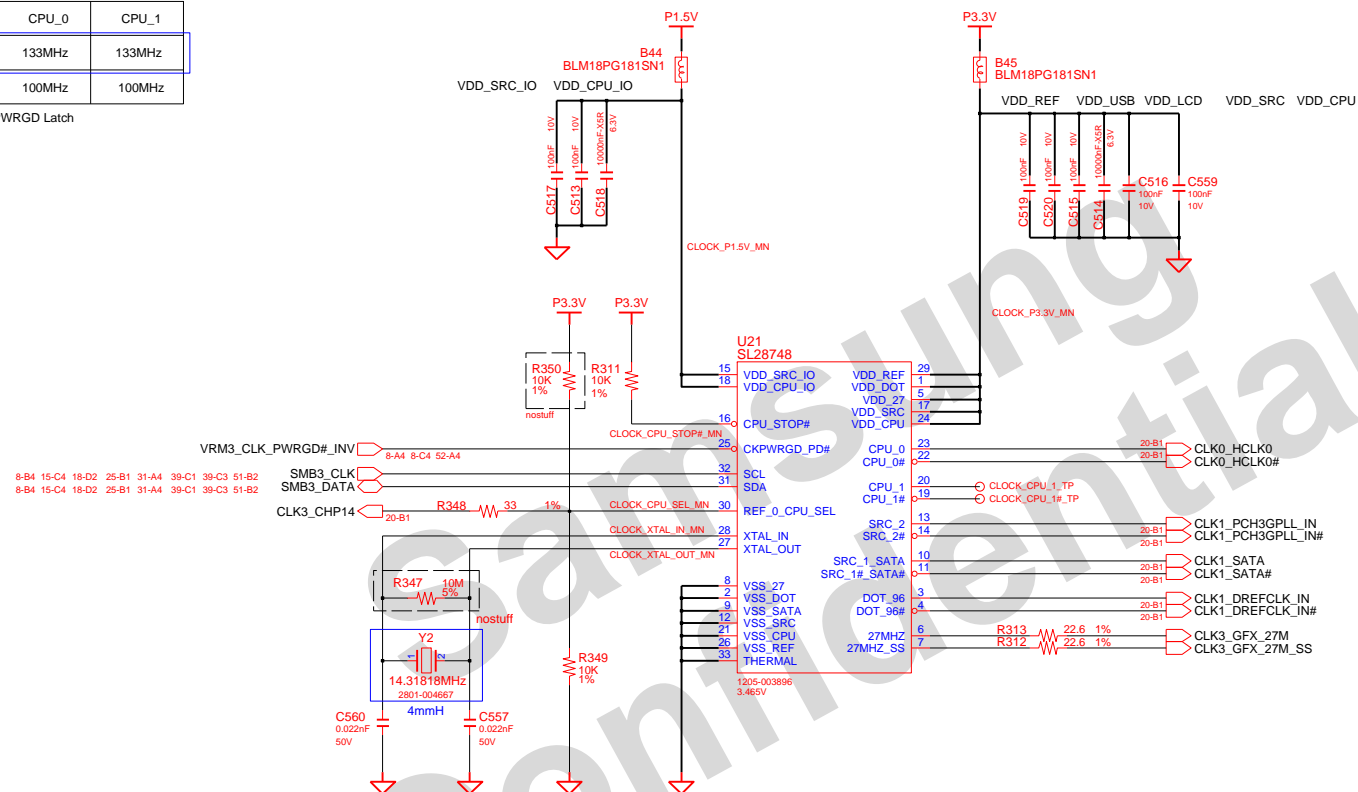
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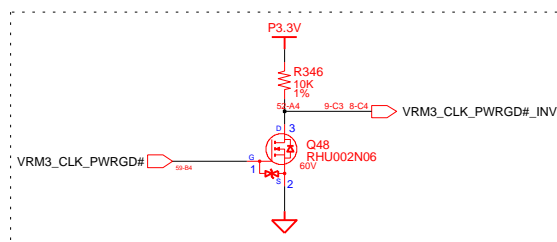
**CK505M SHRINK VERSION****CPU\_MODE SEL**

Pin 30	CPU_0	CPU_1
CPU_SEL = 0	133MHz	133MHz
CPU_SEL = 1	100MHz	100MHz

\*CPU\_SEL During CK\_PWRGD Latch



Place 14.318MHz within  
 500mils of CK-505



DRAW	ZHU, JIAN	DATE	8/12/2006	TITLE	Suzhou2-LA Main_Clock_Circuit CK_Clock_505M	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01190/ March, 3, 2010 8:45:34 PM
CHECK	GUO, LEI	DEV. STEP	PV			
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE		LAST EDIT				

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# THERMAL SENSOR & FAN CONTROL

## ADDRESSSEL MODE

0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb

## SHDN\_SEL MODE

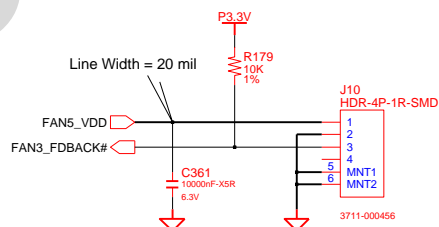
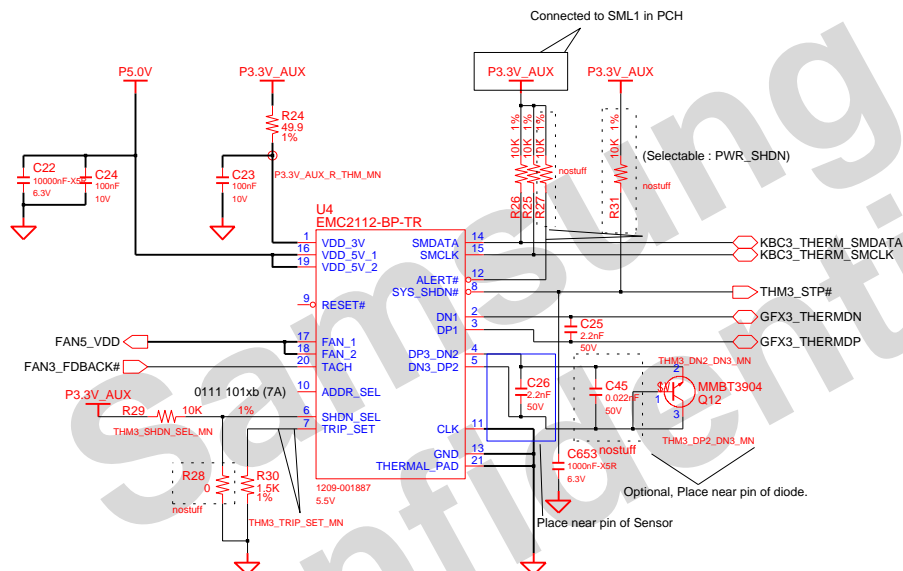
0	INTEL TR MODE
HIGH Z	AMD CPU/DIODE MODE
✓ 1	EXT.DIODE 2 MODE

## TRIP\_SET Resistor Setting ( 60 ~ 122 C)

60	0.0
95	1500
96	1580
97	1690
98	1820
99	1960
100	2050
101	2210
102	2370
✓ 103	2550
104	2740
105	2940
122	49900

$$V\_Trip = (T\_Trip - T\_Min) / 80$$

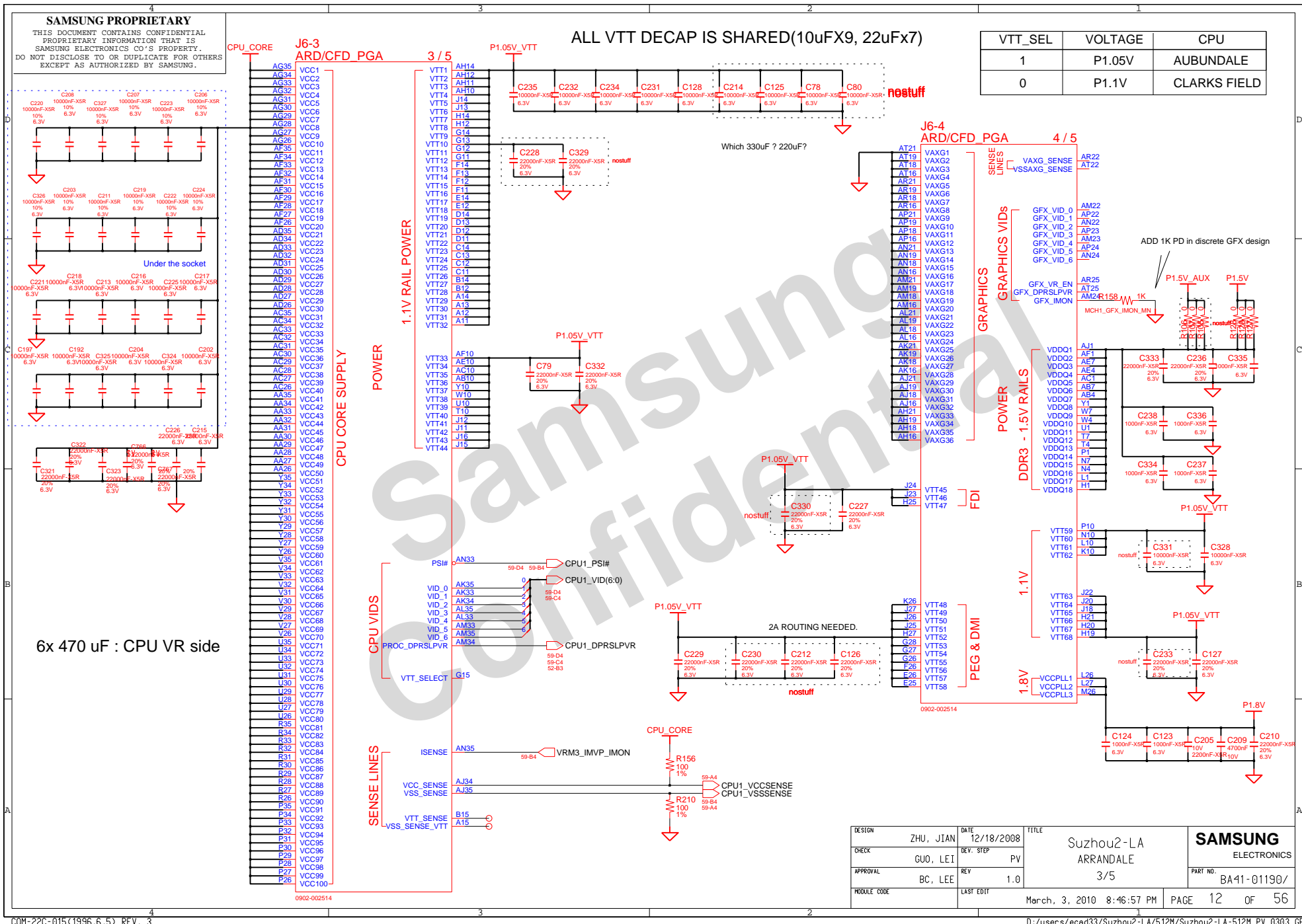
V\_TRIP : TRIP\_SET Voltage  
 T\_Min : Minimum Temperature

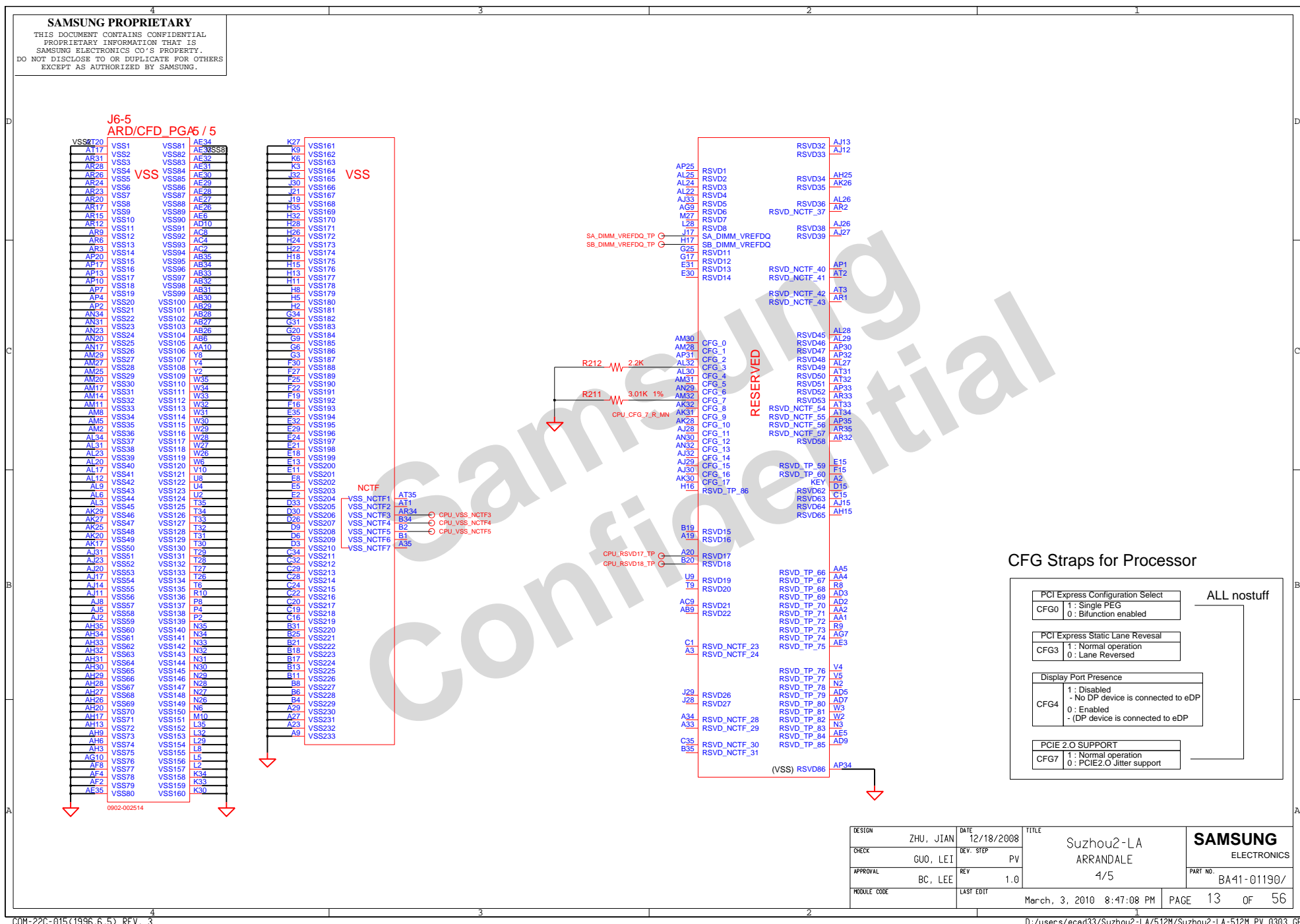


DESIGN	ZHU, JIAN	DATE	3/3/2010	TITLE	Suzhou2-LA THERMAL SENSOR EMC2112	SAMSUNG ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV			
APPROVAL	BC, LEE	REV	1.0			PART NO. BA41-01190/
MODULE CODE		LAST EDIT	March, 3, 2010 8:45:54 PM	PAGE	9 OF 56	

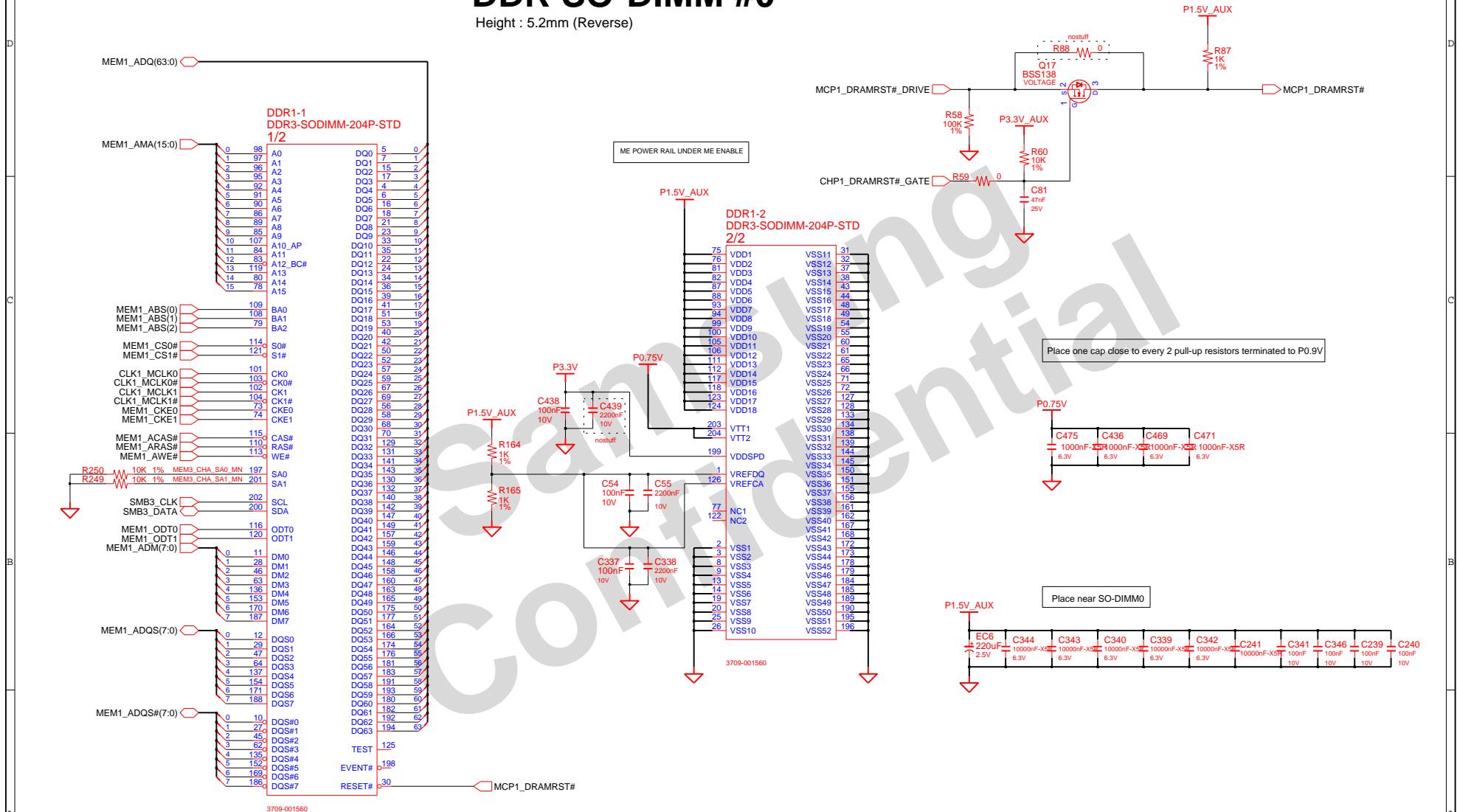









Height : 5.2mm (Reverse)



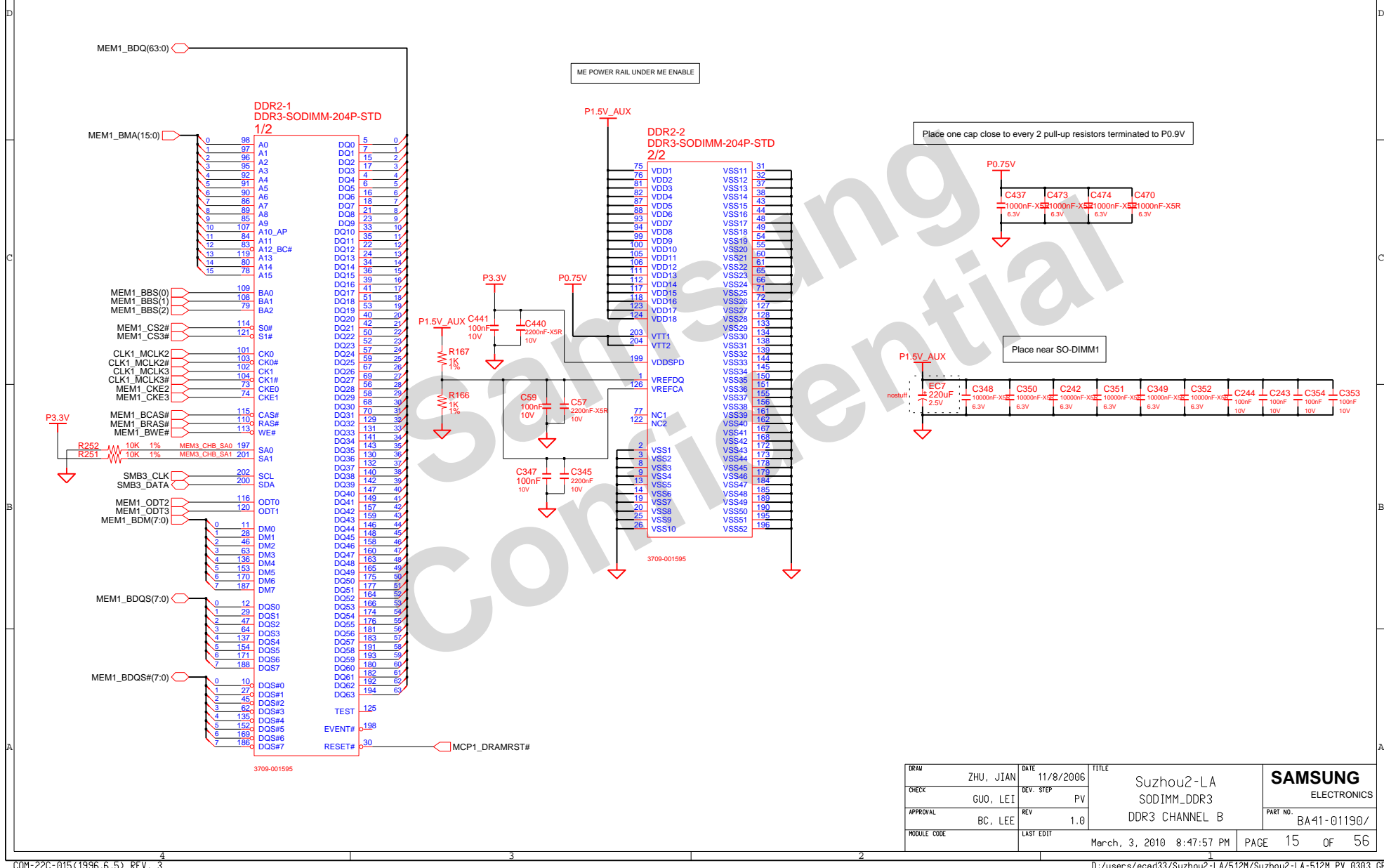
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CHECK	GUO, LEI	DEV. STEP	PV		SODIMM_DDR3	
APPROVAL	BC, LEE	REV	1.0		DDR3 CHANNEL A	
MODULE CODE		LAST EDIT				
				March, 3, 2010 8:47:19 PM	PAGE	14 OF 56

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## DDR SO-DIMM #1

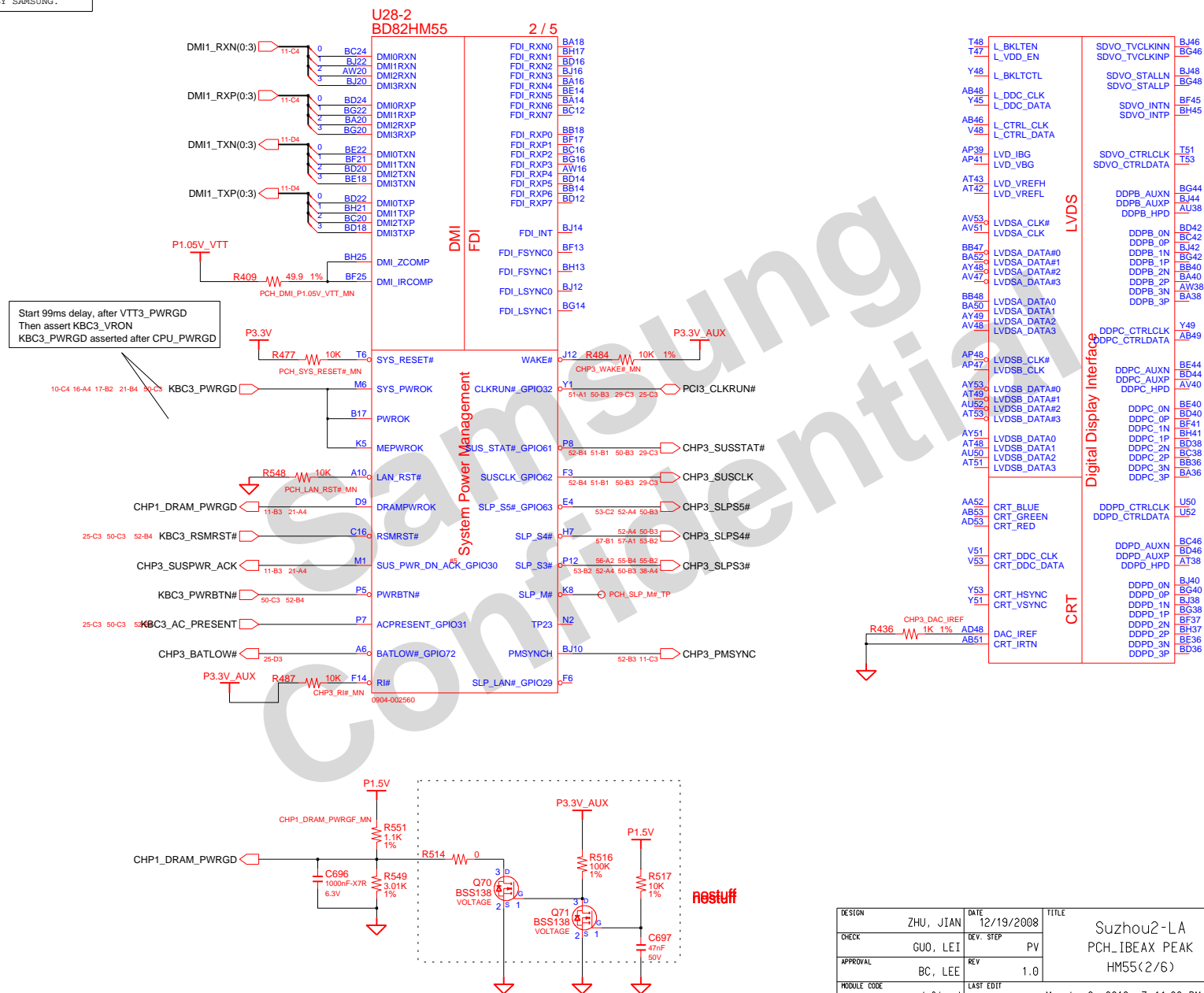
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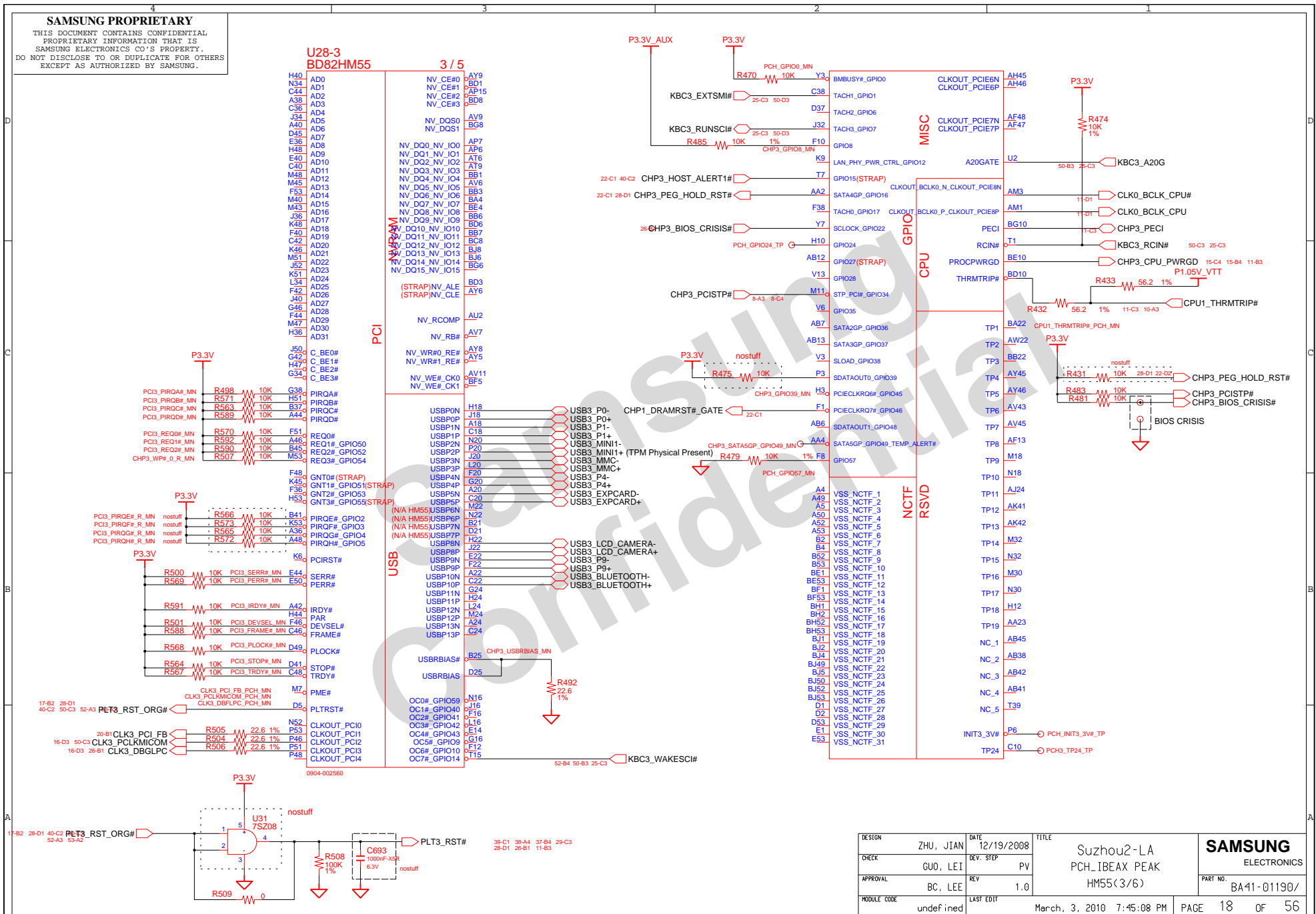








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				PART NO.	BA41-01190/	



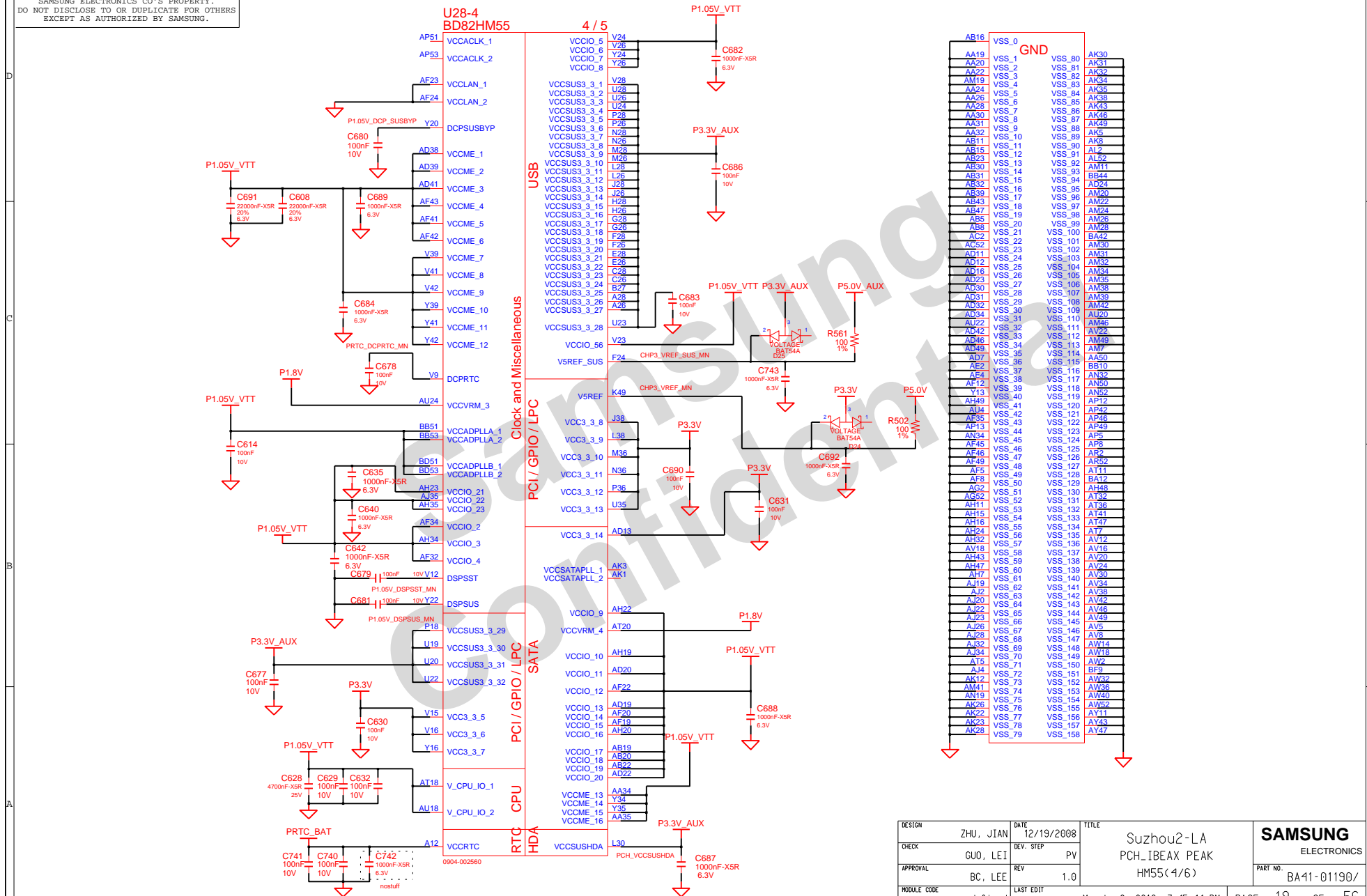
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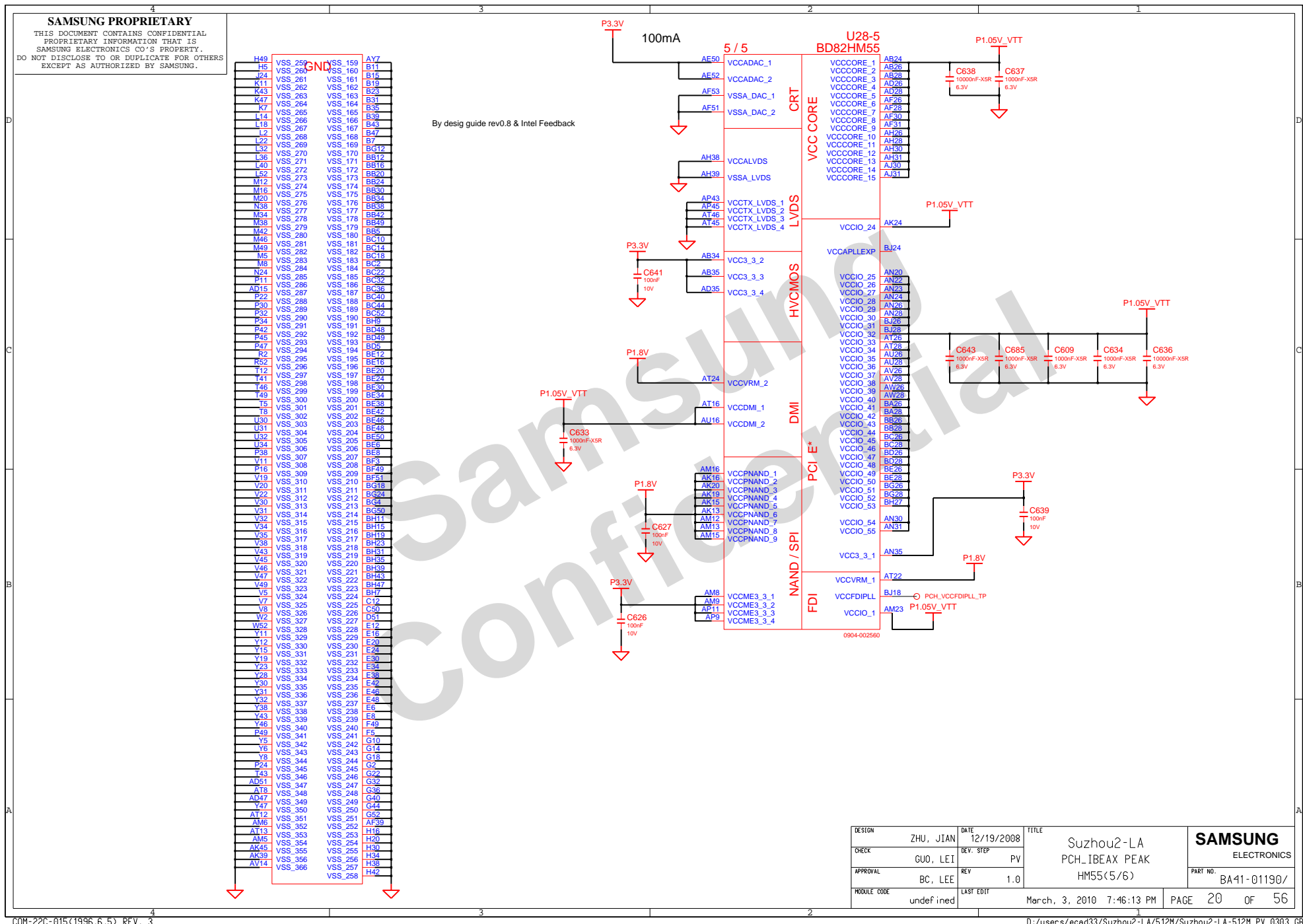
P1.1V,P1.1V\_M is P1.05V &amp; P1.05V\_M ACTUALLY

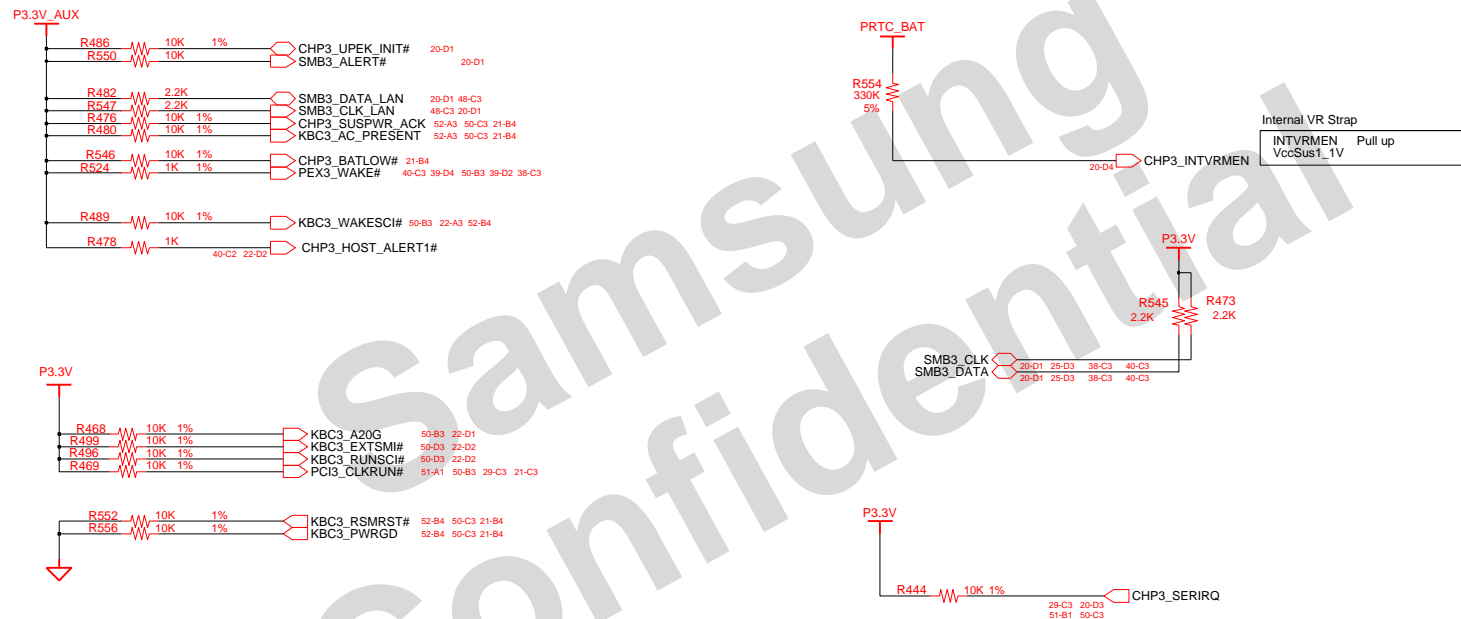
U28-4  
BD82HM55

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DESIGN	ZHU, JIAN	DATE	12/19/2008	TITLE	Suzhou2-LA	SAMSUNG ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV		PCH_IBEAX PEAK	
APPROVAL	BC, LEE	REV	1.0		HM55(4/6)	PART NO.
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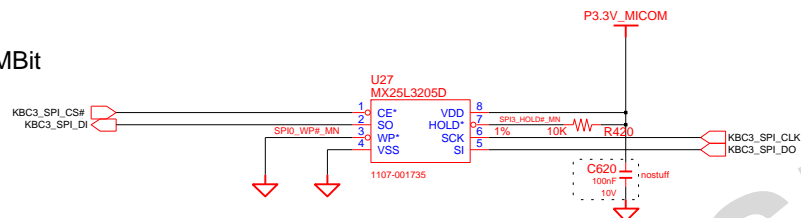
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APPROVAL	BC, LEE	REV	1.0				PART NO.	BA41-01190/
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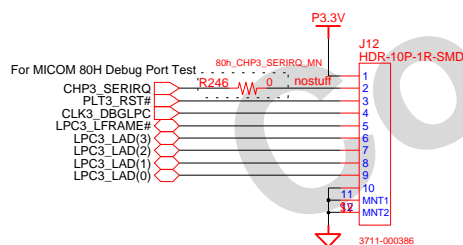
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# SPI\_BIOS\_ROM

32MBit



80H DECODER CONNECTOR



02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT. CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
14	WITH INITIAL POST VALUE	88	INIT. BIOS DATA ROM
16	INIT. KEYBOARD CONTROLLER	8A	INIT. EXTENDED BIOS DATA AREA
18	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
1A	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPEMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AC	ENTER SETUP
34	TEST CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
3D	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
42	INIT. INTERRUPT VECTOR	B7	ACPI INIT
44	INIT. BIOS INTERRUPT	BA	DMI INIT
46	CHECK ROM COPYRIGHT NOTICE	BE	CLEAR SCREEN
47	INIT. I2O SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D0	INTERRUPT HANDLER ERROR
49	INIT. PCI BUS AND DEVICE	D2	UNKNOWN INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
4C	SHADOW VIDEO BIOS ROM	D6	SHUTDOWN 2
50	DISPLAY CPU TYPE AND SPEED	D8	SHUTDOWN ERROR
52	TEST KEYBOARD	DA	EXTENDED BLOCK MOVE
54	SET KEYCLICK IF ENABLED	DC	SHUTDOWN 10
56	ENABLE KEYBOARD	E0	ENABLE NMI
58	TEST FOR UNEXPECTED INTERRUPTS	90	INIT. HDD CONTROLLER
5A	DISPLAY * PRESS ..... SETUP	91	INIT. LOCAL BUS HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	92	JUMP TO USER PATCH 2
60	TEST EXTENDED MEMORY	94	DISABLE A20 ADDRESS LINE
62	TEST EXTENDED MEMORY ADDRESS LINE	96	CLEAR HUGE ES SEGMENT REG.
64	JUMP TO USER PATCH 1	98	SEARCH FOR OPTION ROMS

DRAW	ZHU, JIAN	DATE	8/12/2006	TITLE	Suzhou2-LA	SAMSUNG ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV		SPI_BIOS_ROM	
APPROVAL	BC, LEE	REV	1.0		SPI_BIOS_ROM	
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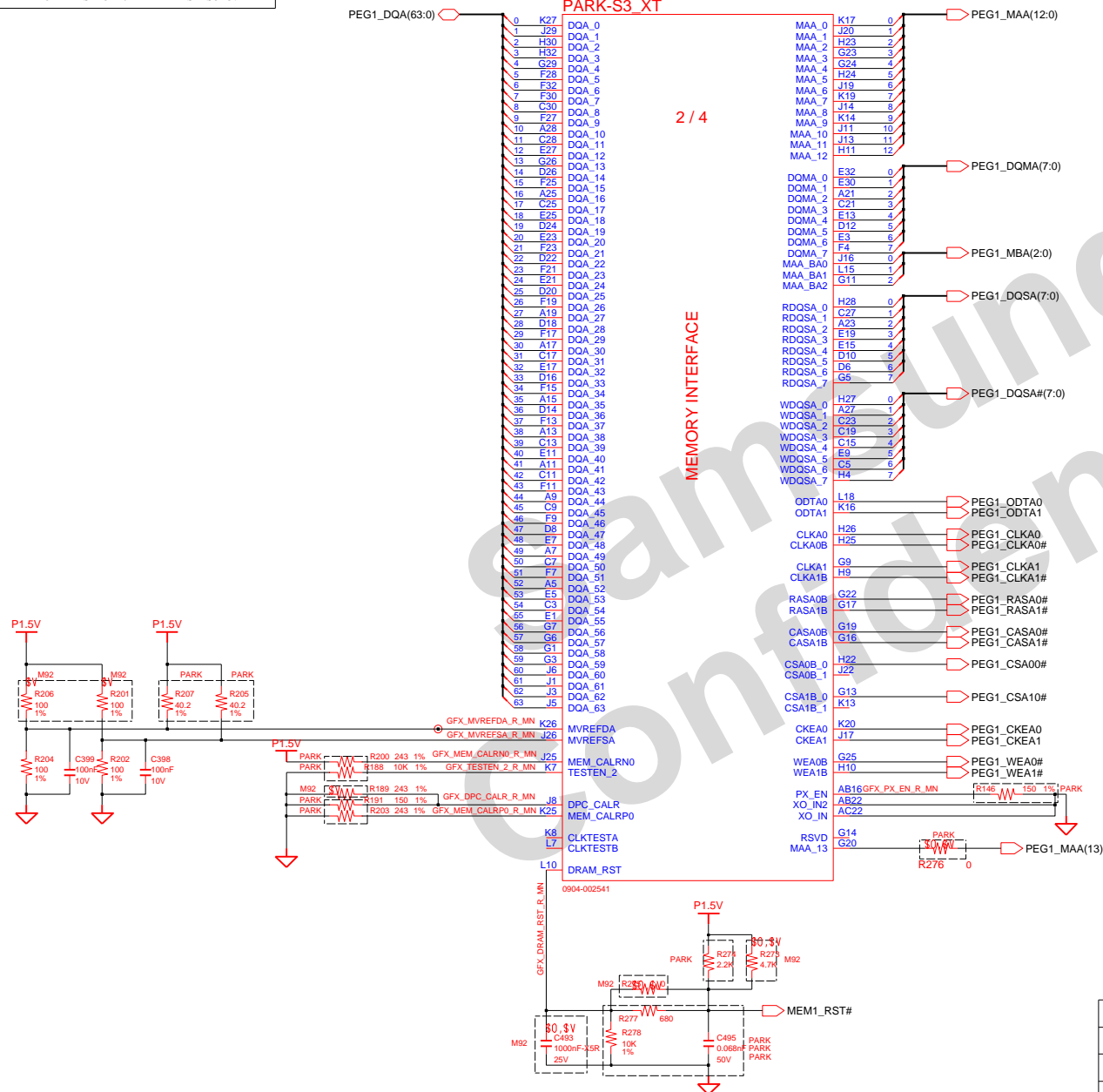
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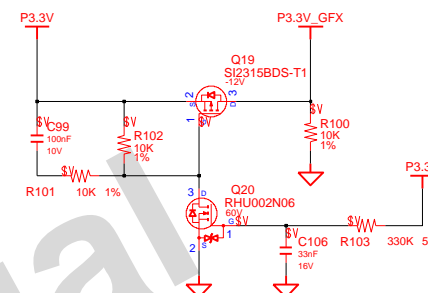
U10-2  
PARK-S3\_XT

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MEMORY INTERFACE



## P3.3V\_GFX CONTROL CIRCUIT FOR M92



	R273	R275	C493	
M92-S2	4.7K,2007-000143	0ohm,2007-000171	1000nF 2203-006348	
PARK-S3	NOSTUFF	NOSTUFF	NOSTUFF	
	R277	R274	R277	C495
M92-S2	NOSTUFF	NOSTUFF	NOSTUFF	NOSTUFF
PARK-S3	10K,2007-007142	2.2K,2007-000141	680ohm 2007-001119	68pF 2203-001156

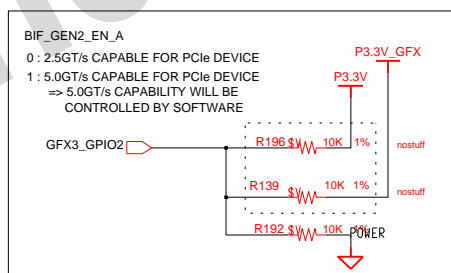
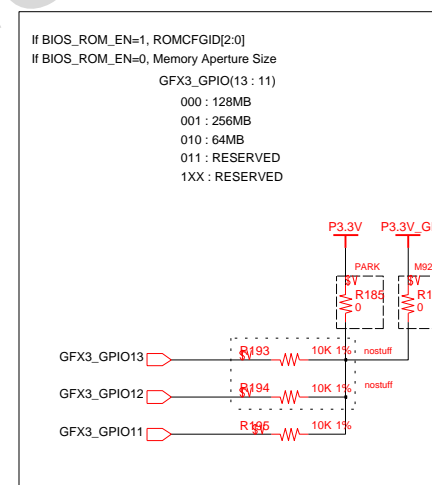
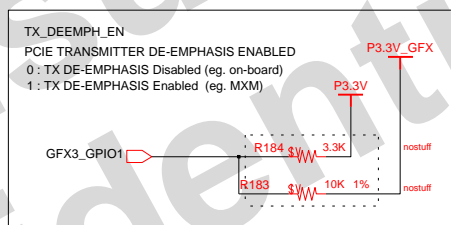
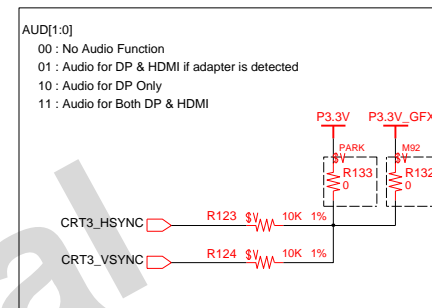
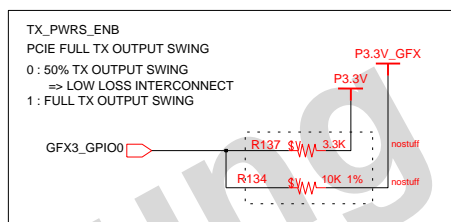
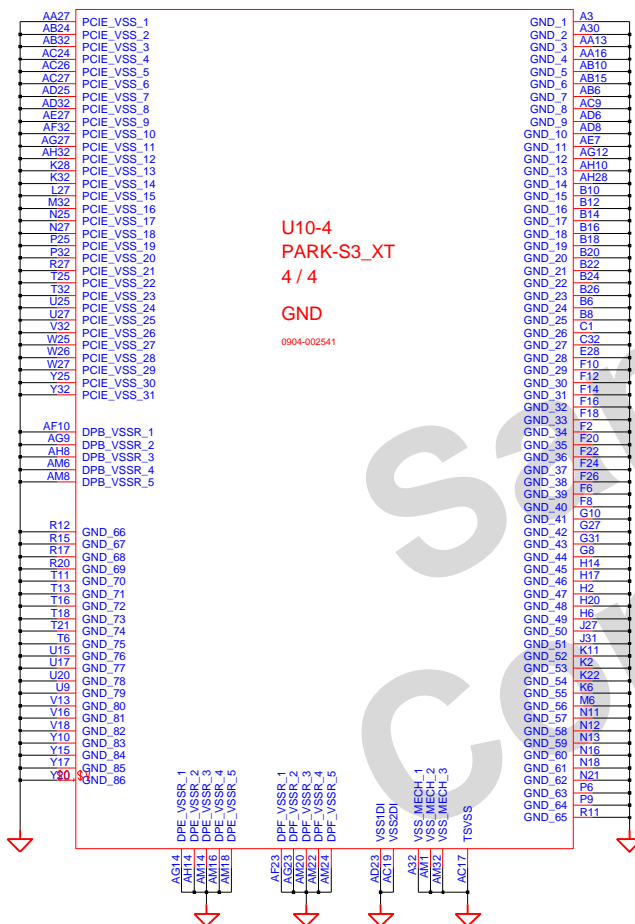
DRAW	ZHU, JIAN	DATE	08/18/2009	Suzhou2-LA  GFX  PARK-S3_XT (2/4)		SAMSUNG ELECTRONICS			
CHECK	GUO, LEI	DEV. STEP	PV						
APPROVAL	BC, LEE	REV	1.0						
MODULE CODE	LAST EDIT		March, 3, 2010 7:49:29 PM			PAGE	24	OF	56





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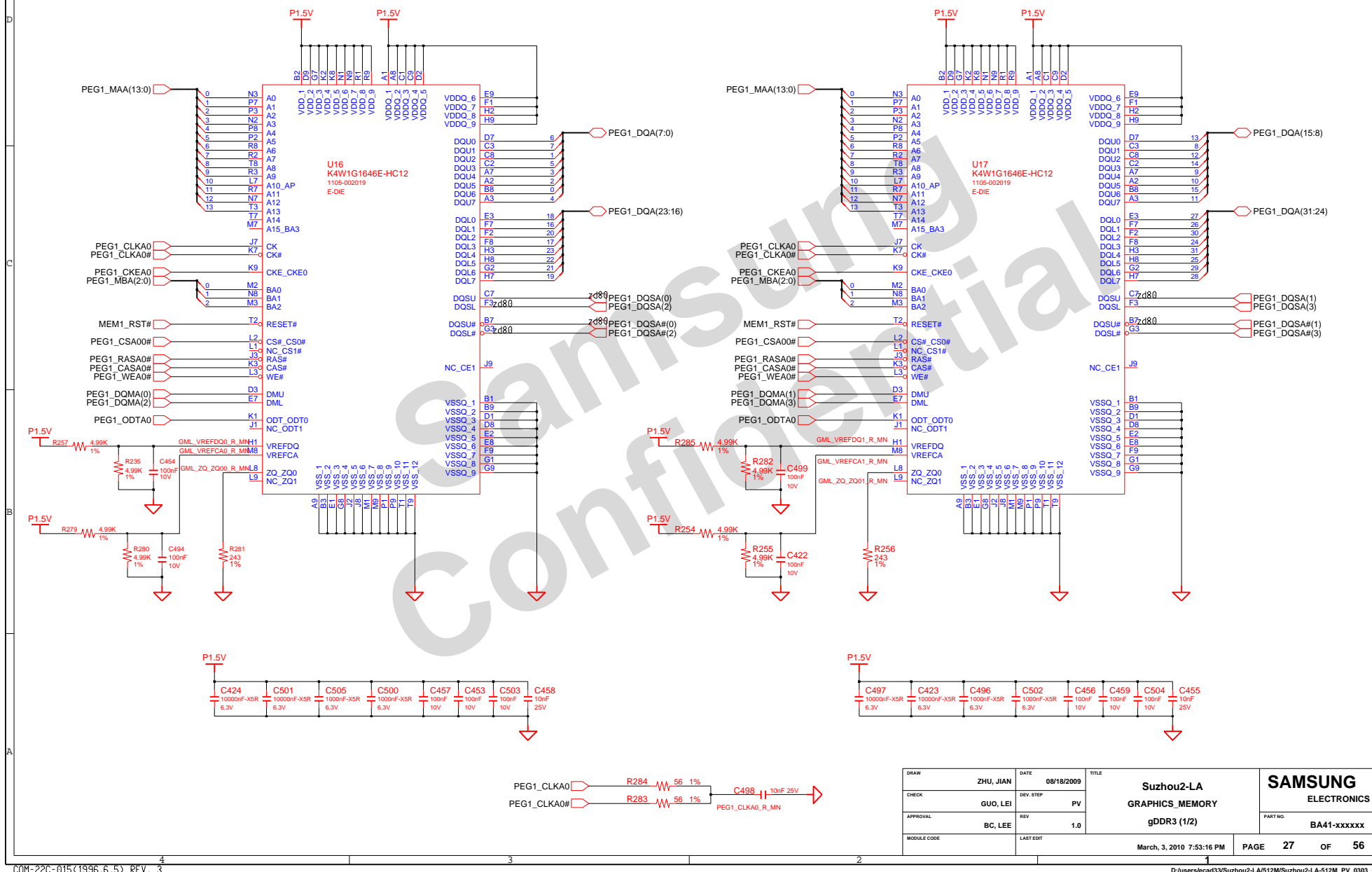
**PARK & M92 Straps**

DRAW	ZHU, JIAN	DATE	08/18/2009	TITLE	Suzhou2-LA	<b>SAMSUNG</b> ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV		GFX	
APPROVAL	BC, LEE	REV	1.0		PARK-S3_XT (4/4)	
MODULE CODE		LAST EDIT		March, 3, 2010 7:51:15 PM	PAGE 26 OF 56	PART NO. BA41-xxxxxx

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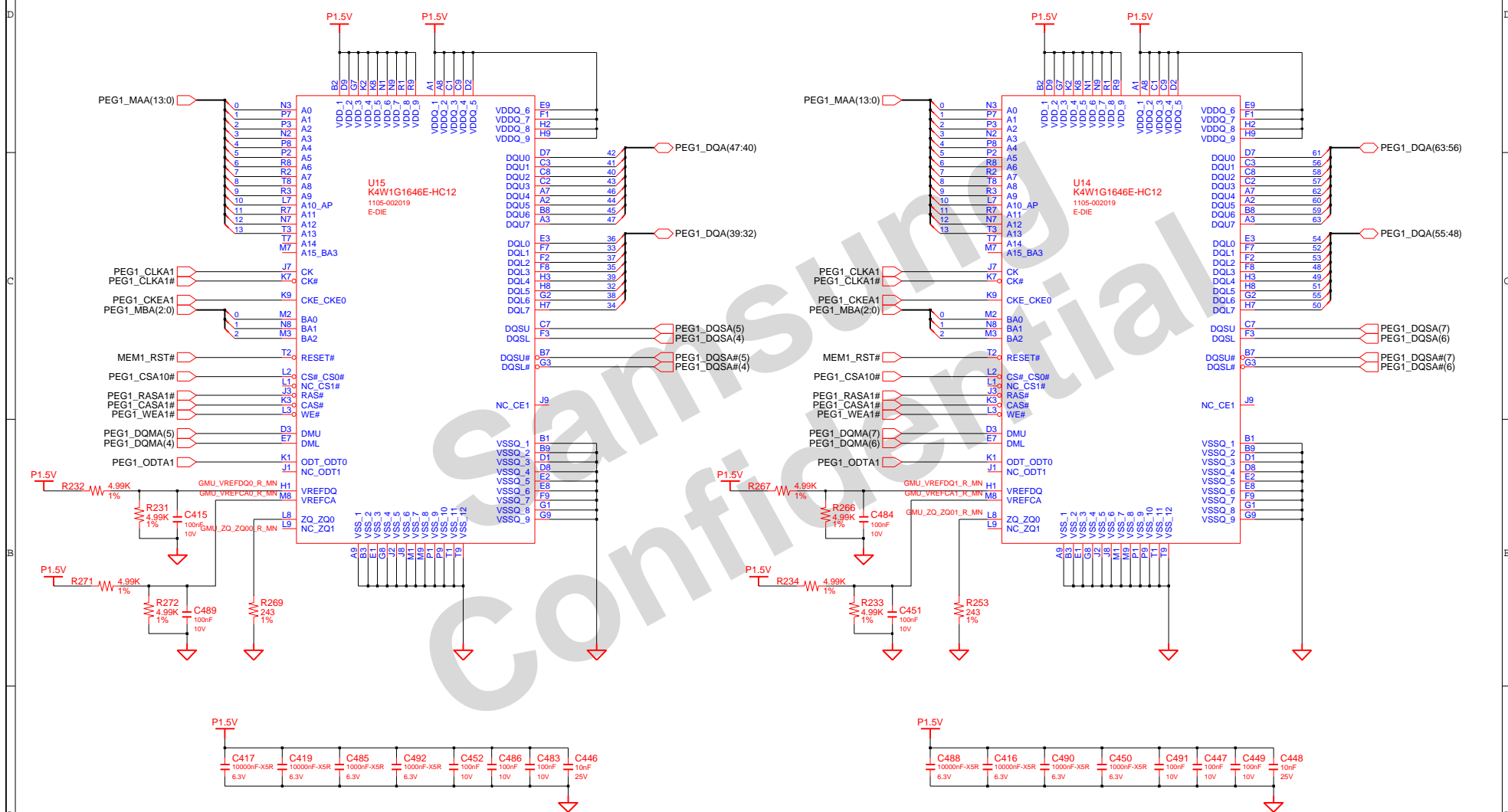
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## A-channel Lower Data



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**A-channel Upper Data**

PEG1\_CLKA1  $\rightarrow$  R268  $\rightarrow$  56 1%  $\rightarrow$  C487  $\rightarrow$  10nF 25V  $\rightarrow$   
 PEG1\_CLKA1#  $\rightarrow$  R270  $\rightarrow$  56 1%  $\rightarrow$  PEG1\_CLKA1\_R\_MN

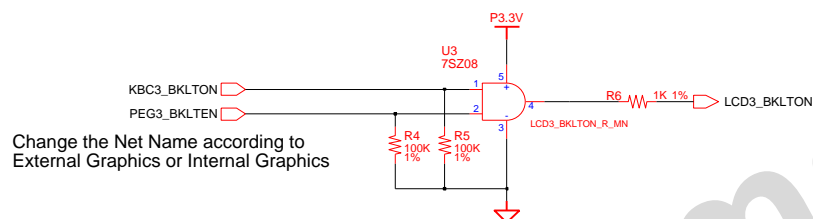
DRAW	ZHU, JIAN	DATE	08/18/2009	TITLE	Suzhou2-LA	SAMSUNG ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV		GRAPHICS_MEMORY	
APPROVAL	BC, LEE	REV	1.0		gDDR3 (2/2)	
MODULE CODE		LAST EDIT				
March, 3, 2010 7:54:22 PM						PAGE 28 OF 56

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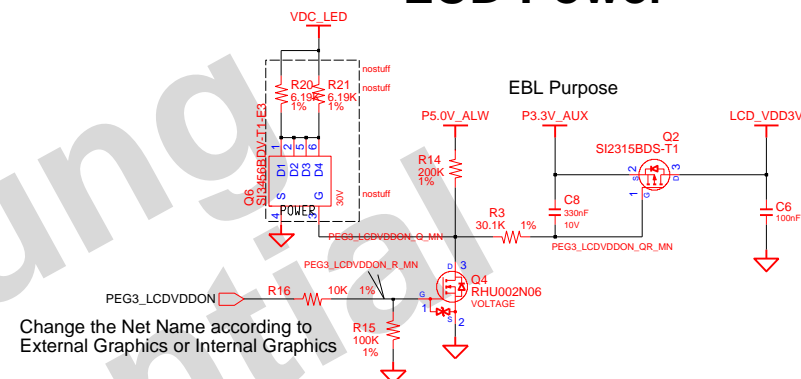
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# LVDS

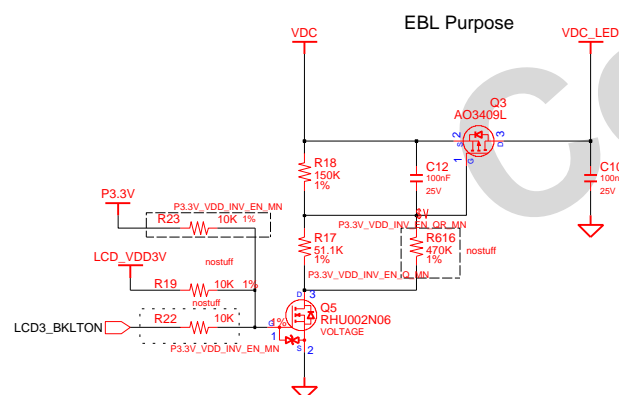
## Backlight On



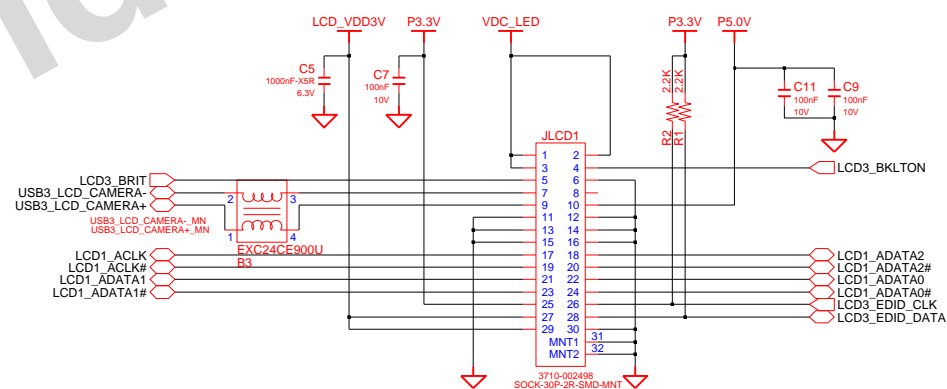
## LCD Power



## Converter Power



## 1Ch. LCD Connector



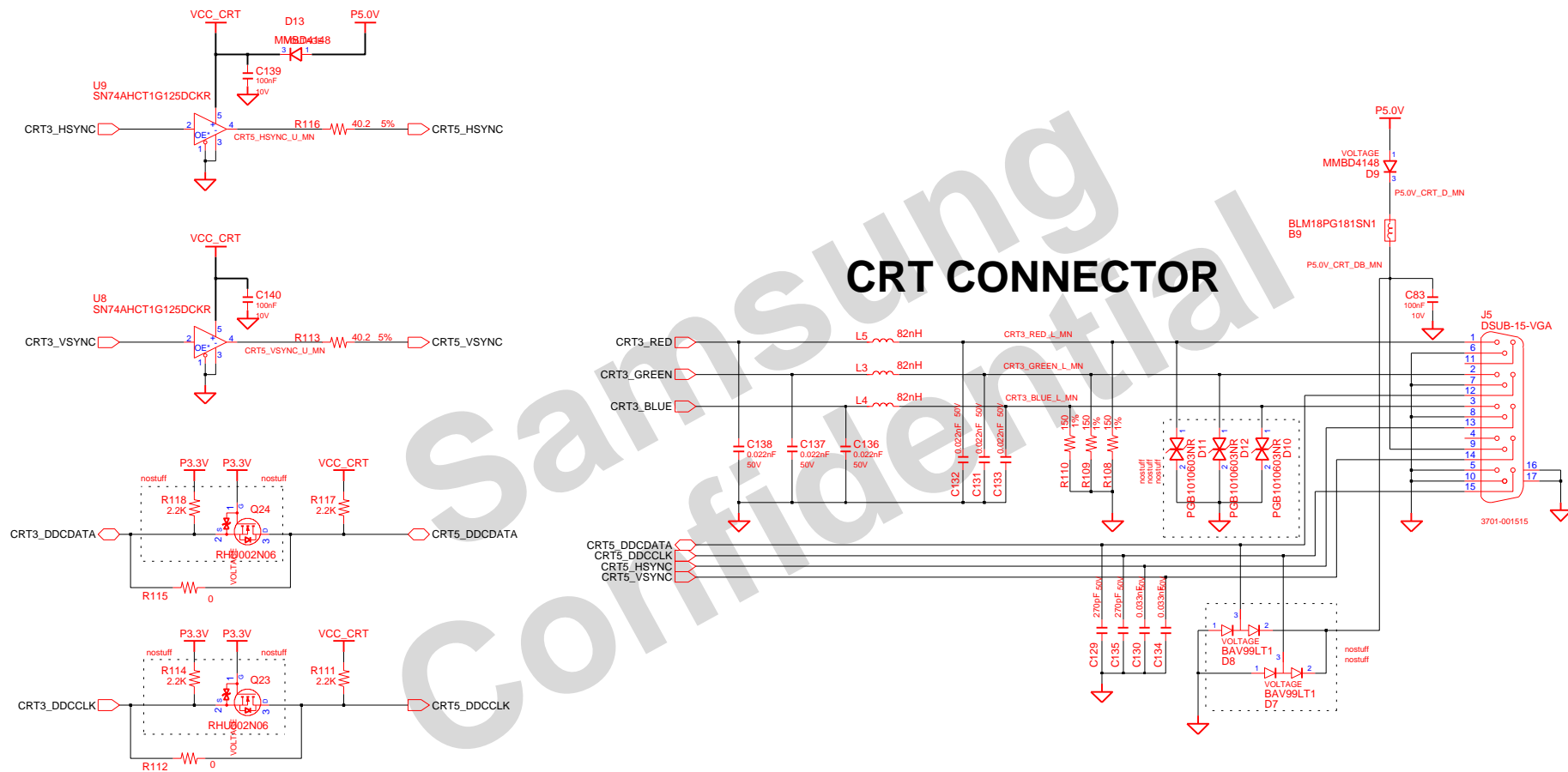
DESIGN	ZHU, JIAN	DATE	01/08/2009	TITLE	Suzhou2-LA GRAPHICS_IF LVDS	<b>SAMSUNG</b> ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV			PART NO. BA41-01190/
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 7:54:52 PM	PAGE	29	OF 56

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# CRT

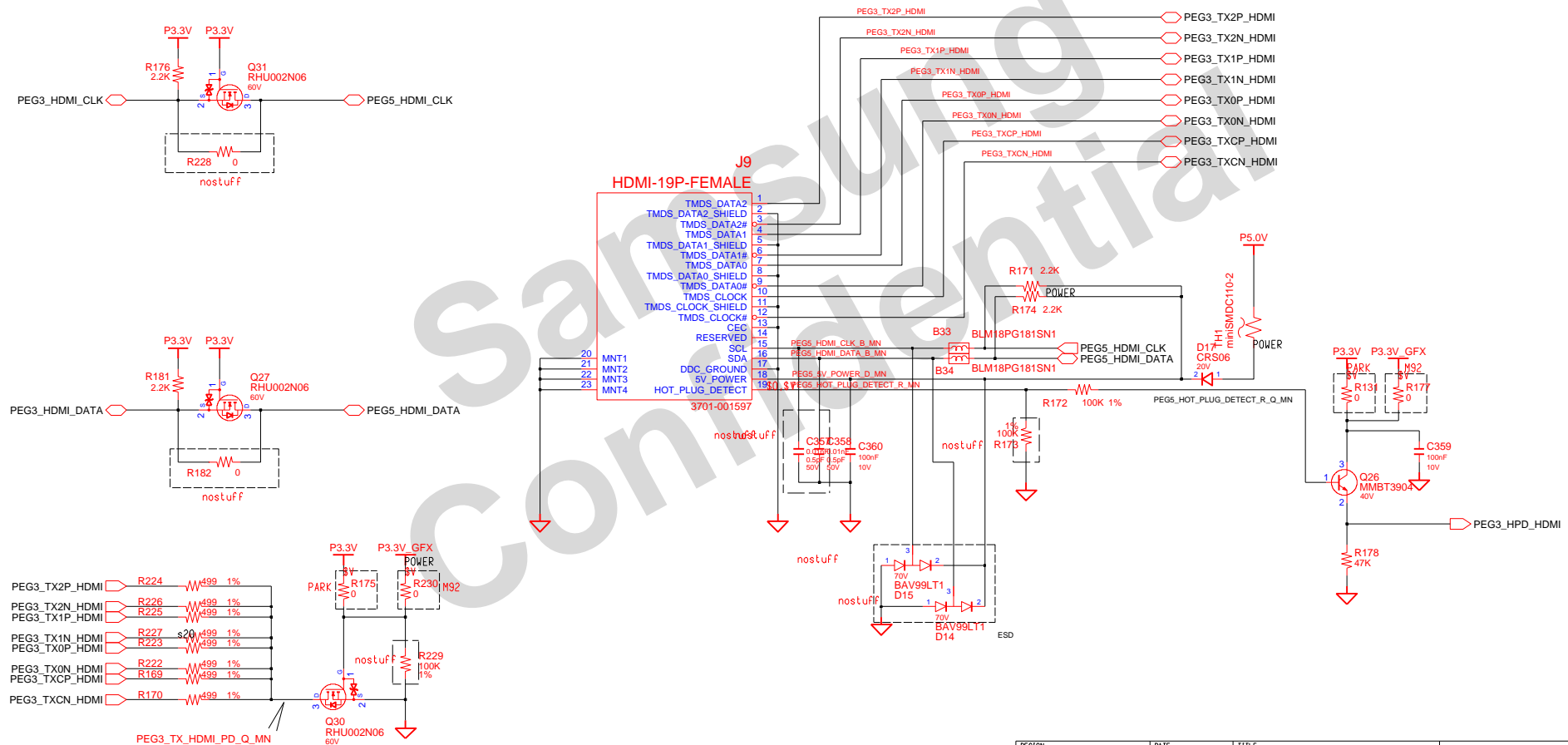
## CRT CONNECTOR



Check "CRT3\_DDCCLK/DATA" Voltage Level  
 2N06 Can be replaced with SM6K2

DESIGN	ZHU, JIAN	DATE	01/08/2009	TITLE	Suzhou2-LA GRAPHICS_IF CRT	<b>SAMSUNG</b> ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV			PART NO. BA41-01190/
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 7:55:58 PM	PAGE	30	OF 56

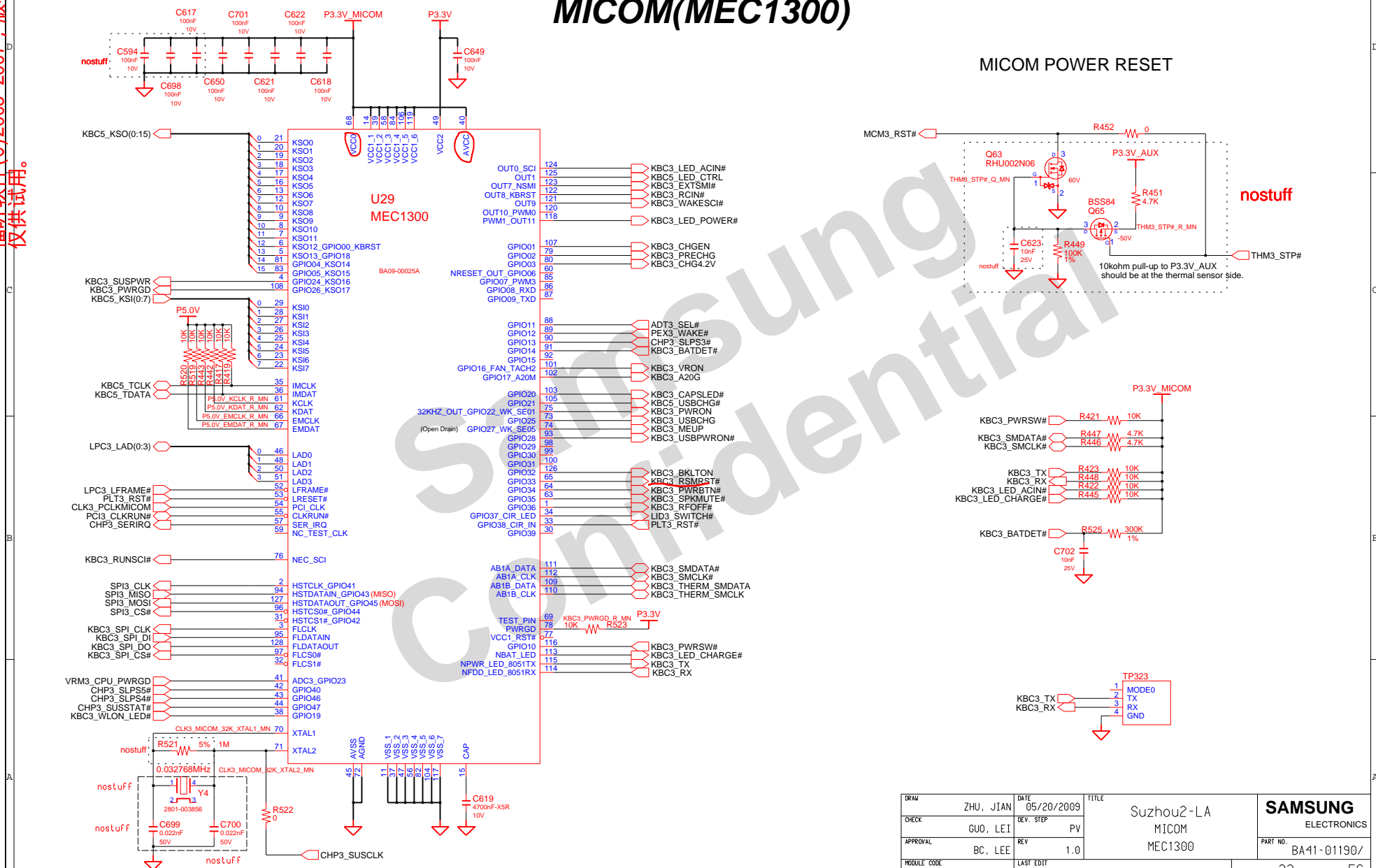
FOR HDMI VERIFICATION TEST



DESIGN	ZHU, JIAN	DATE	8/14/2009	TITLE	Suzhou2-LA GRAPHICS_1F	<b>SAMSUNG</b> ELECTRONICS	
CHECK	GUO, LEI	DEV. STEP	PV			PART NO.	
APPROVAL	BC, LEE	REV	1.0	HDMI		BA41-xxxxxA	
MODULE CODE	undefined	LAST EDIT		March, 3, 2010 7:57:00 PM	PAGE	31	OF 56

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## MICOM POWER RESET



DATE	05/20/2009	TITLE Suzhou2-LA MICOM MEC1300		<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01190/	
DRAW	ZHU, JIAN				
CHECK	GUO, LEI				
DEV. STEP	PV	REV		1.0	
APPROVAL	BC, LEE				
MODULE CODE	LAST EDIT		March, 3, 2010 7:58:19 PM		PAGE 32 OF 56

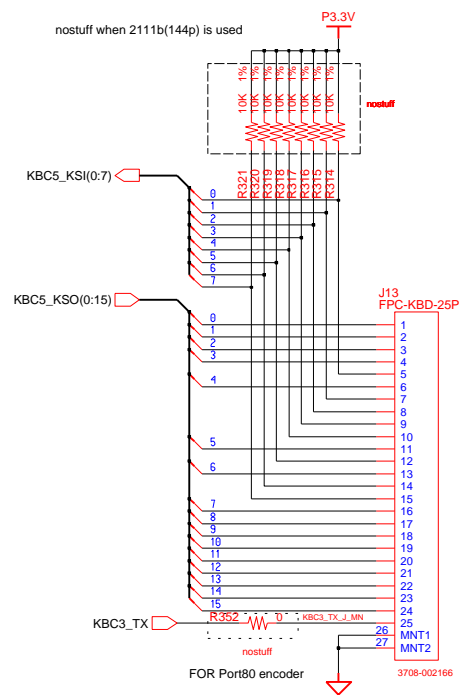


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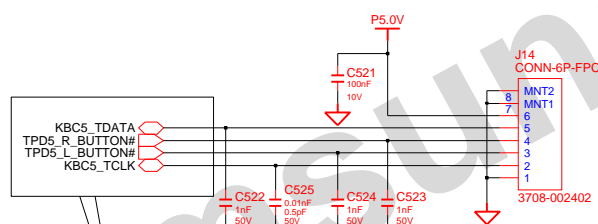
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# Micom Glue Logic

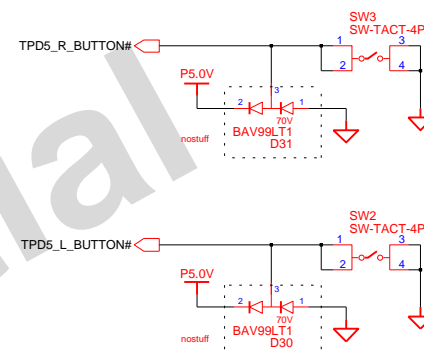
## KEYBOARD



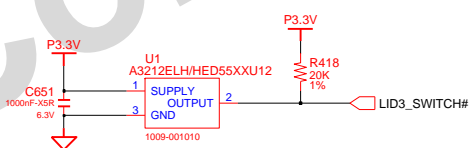
## TOUCHPAD



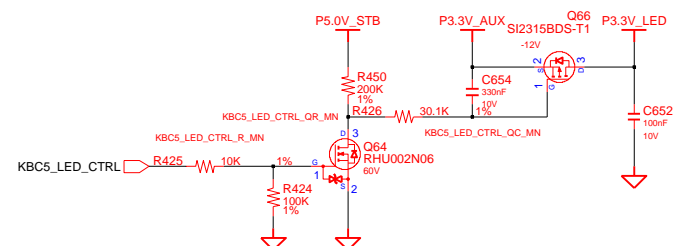
## TOUCHPAD BUTTON



## LID\_SWITCH

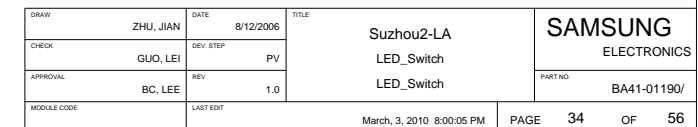


## TOUCHPAD LED POWER



DESIGN	ZHU, JIAN	DATE	6/27/2008	TITLE	Suzhou2-LA MICOM_GLU KBD&TOUCHPAD&L ID	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01190/
CHECK	GUO, LEI	DEV. STEP	PV			
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 7:59:33 PM	PAGE	33 OF 56	

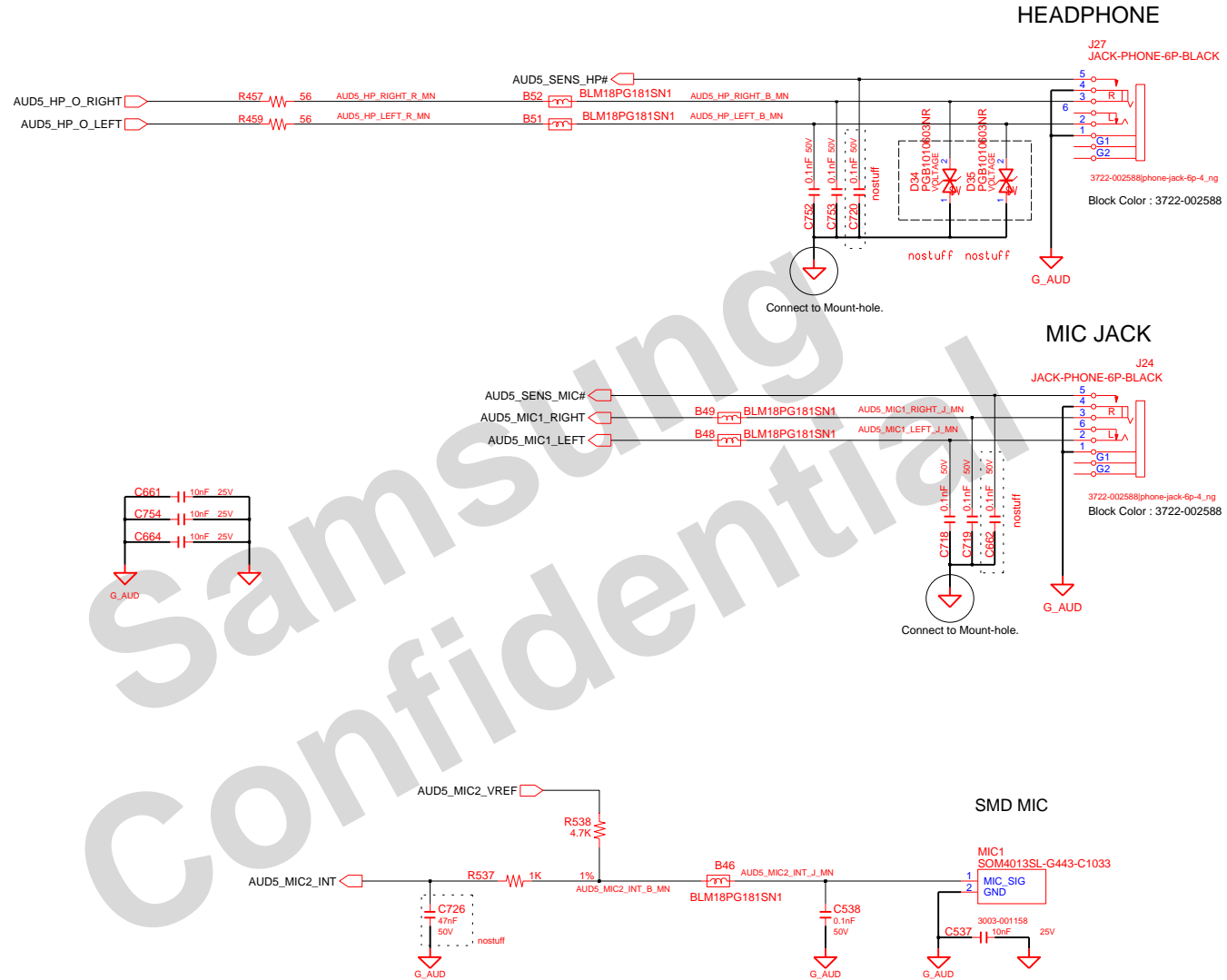
## TOUCHPAD LEDS





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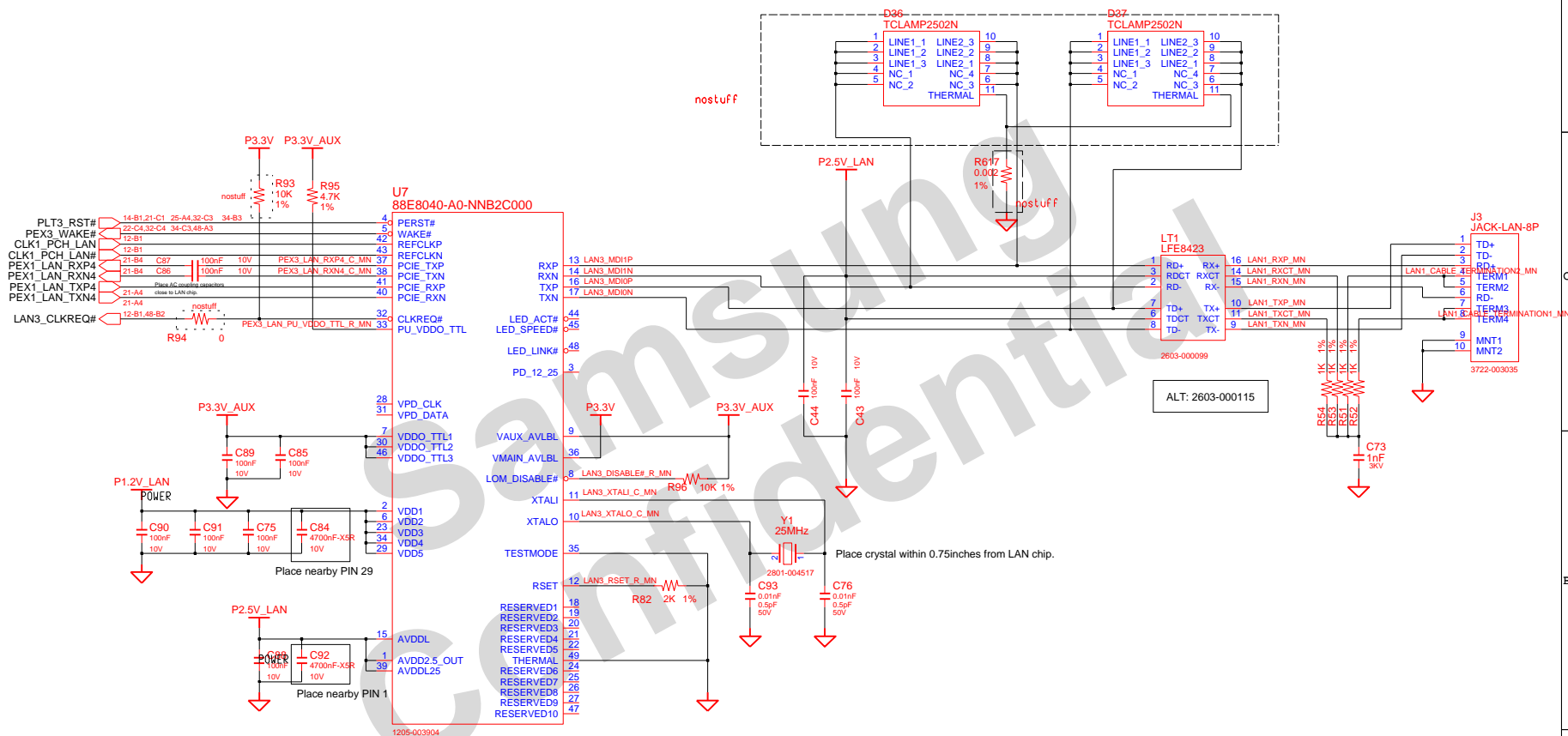


DESIGN	ZHU, JIAN	DATE	3/13/2009	TITLE	Suzhou2-LA	<b>SAMSUNG</b> ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV		HDA_ALC269Q-VB2	
APPROVAL	BC, LEE	REV	1.0		AUDIO INPUT/OUTPUT	
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 8:03:23 PM	PAGE	36 OF 56	

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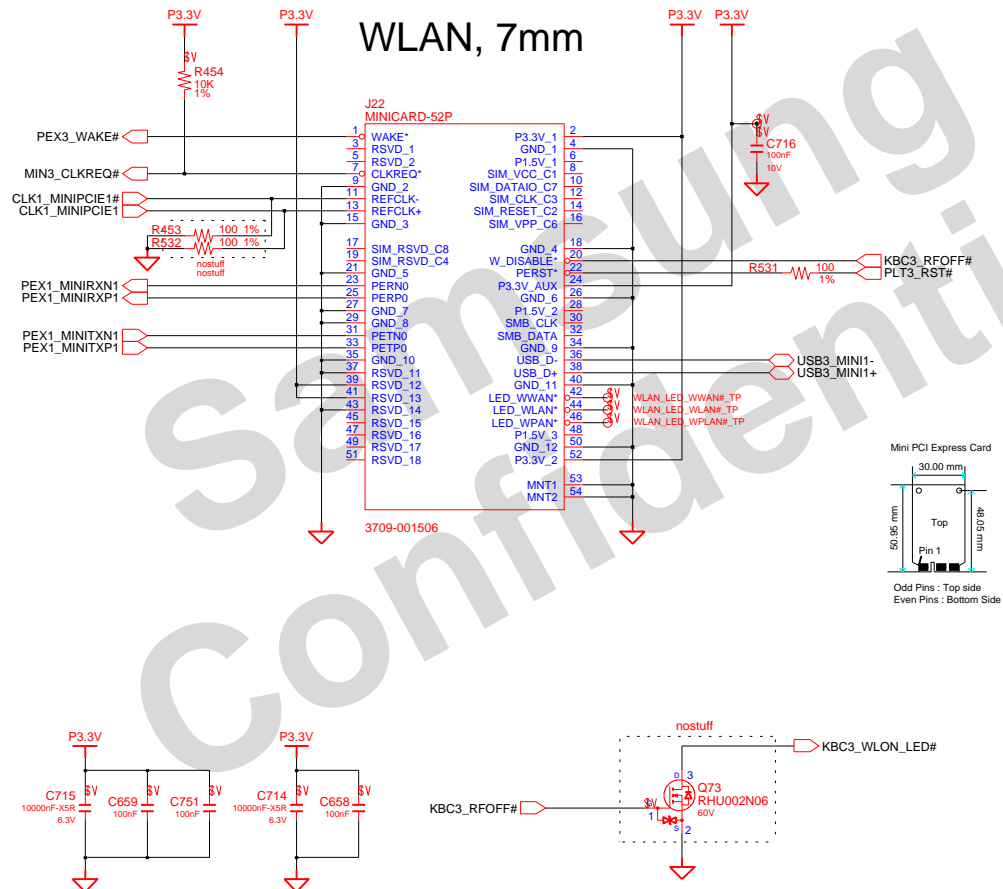
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# LAN Controller (Marvell 88E8040)



DESIGN	ZHU, JIAN	DATE	10/6/2008	TITLE	Suzhou2-LA LAN Marvell 88E8040	SAMSUNG ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV			PART NO. BA41-01190/
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 8:05:58 PM	PAGE	37	OF 56

## WLAN, 7mm



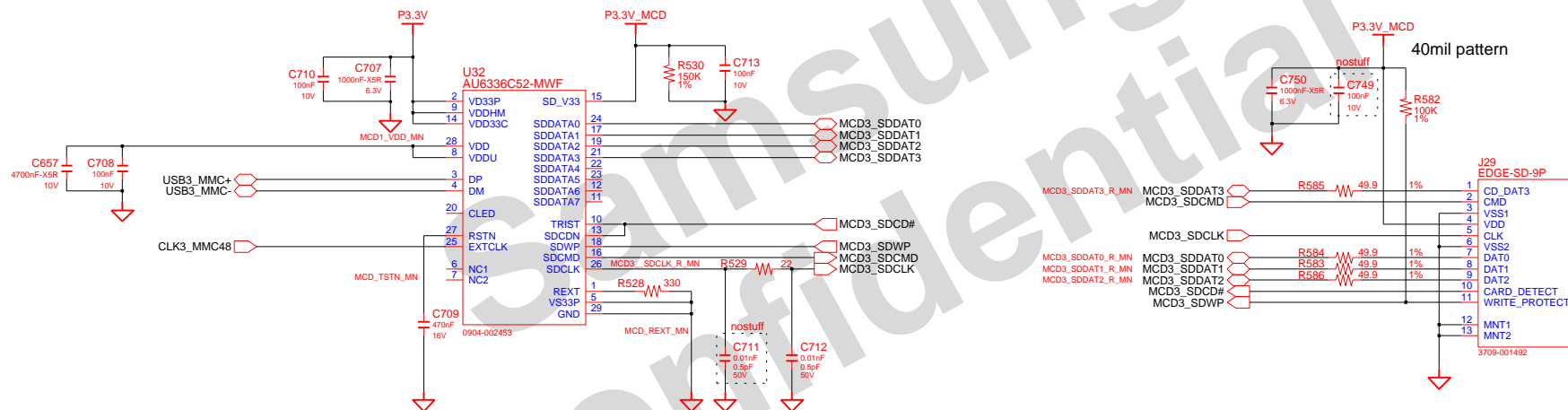
DESIGN	ZHU, JIAN	DATE	6/6/2008	TITLE Suzhou2-LA MINI_PCIE_CONN Wireless LAN		<b>SAMSUNG</b> ELECTRONICS	
CHECK	GUO, LEI	DEV. STEP	PV				
APPROVAL	BC, LEE	REV	1.0				
MODULE CODE		LAST EDIT		March, 3, 2010 8:07:00 PM	PAGE	38	OF 56

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# Card Reader (AU6336)

P3.3V\_MCD distance between R5U880 and socket should be less than 2 inches



40 mil trace for medica card socket ground

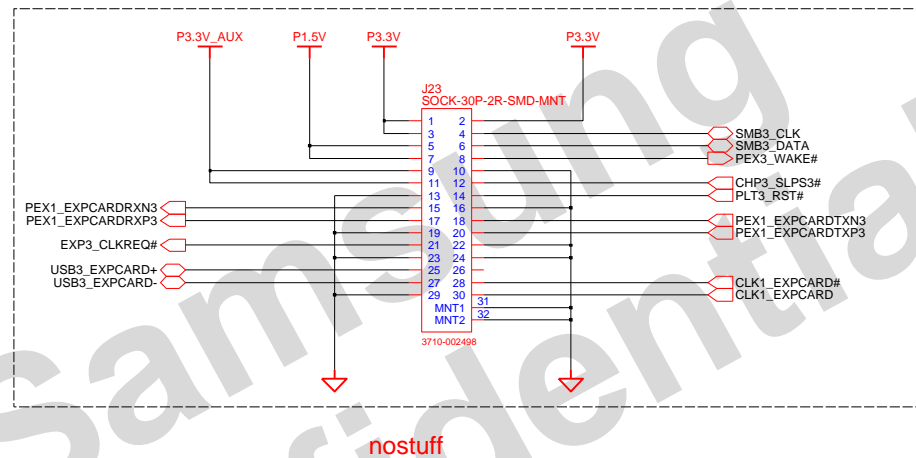
MSEL5	SD Write Protec Selection
Connected to VCC	High Enable
Connected to GND	Low Enable
MSEL7	PLL BASE CLOCK SELECTION
Connected to VCC	12MHz
Connected to GND	48MHz

DESIGN	ZHU, JIAN	DATE	10/15/2008	TITLE	Suzhou2-LA	<b>SAMSUNG</b> ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV		MULTICARD	
APPROVAL	BC, LEE	REV	1.0		AU6336	
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 8:08:12 PM	PAGE	39 OF 56	

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# Express Card



DESIGN	ZHU, JIAN	DATE	7/7/2008	TITLE	Suzhou2-LA EXPRESS CARD	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01190/
CHECK	GUO, LEI	DEV. STEP	PV			
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 8:09:12 PM	PAGE	40 OF 56	

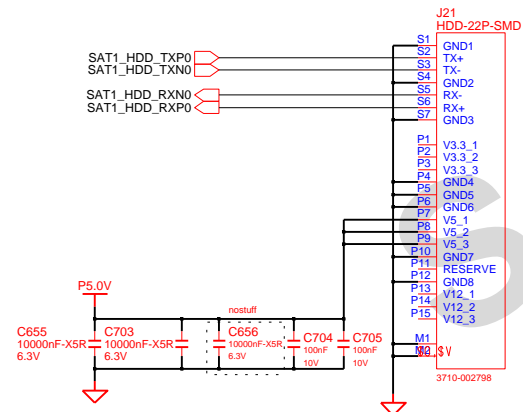


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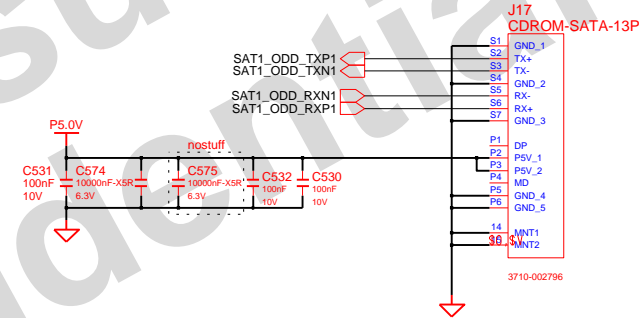
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# SATA I/F CONN

SATA HDD CONN



SATA ODD CONN



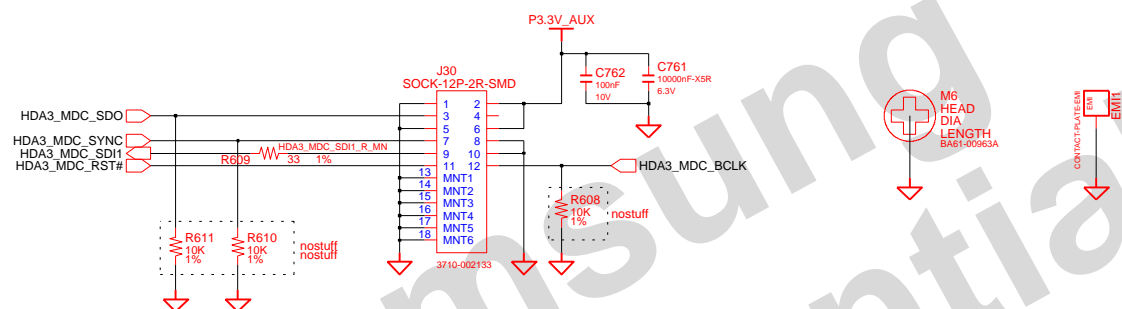
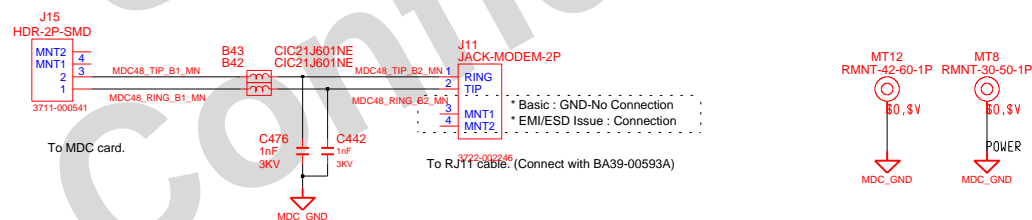
DESIGN	ZHU, JIAN	DATE	6/6/2008	TITLE	Suzhou2-LA SATA_DEVICES HDD&ODD	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01190/
CHECK	GUO, LEI	DEV. STEP	PV			
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 8:09:40 PM	PAGE	41 OF 56	

**nostuff**

DRAW	ZHU, JIAN	DATE	08/18/2009	Suzhou-2-LA e-SATA	SAMSUNG ELECTRONICS		
CHECK	GUO, LEI	DEV. STEP	PV				
APPROVAL	BC, LEE	REV	1.0				
PART NO.			BA41-xxxxxx				
MODULE CODE	LAST EDIT		March, 3, 2010 8:11:06 PM		PAGE	42	OF 56

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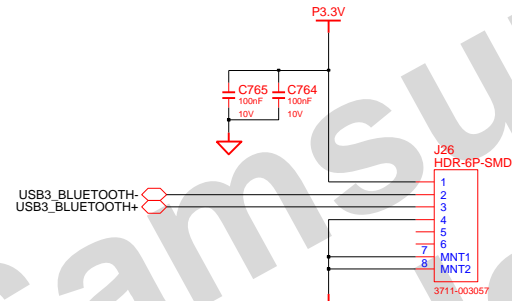
**MDC CONNECTOR****MDC SUB**

DESIGN	ZHU, JIAN	DATE	8/20/2009	TITLE	Suzhou2-LA HDA_MODEM MODEM	<b>SAMSUNG</b> ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV			
APPROVAL	BC, LEE	REV	1.0			PART NO. BA41-01190/
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 8:12:34 PM	PAGE	43	OF 56

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# BLUETOOTH INTERFACE



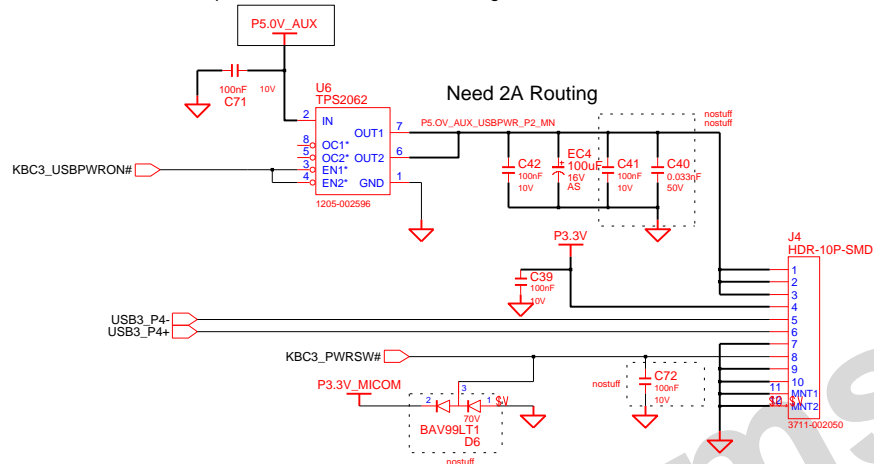
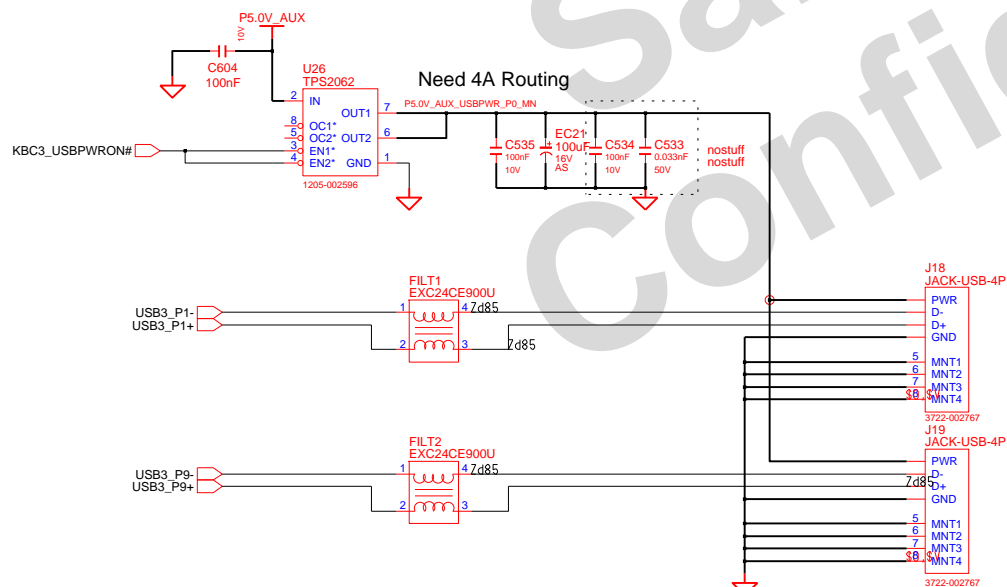
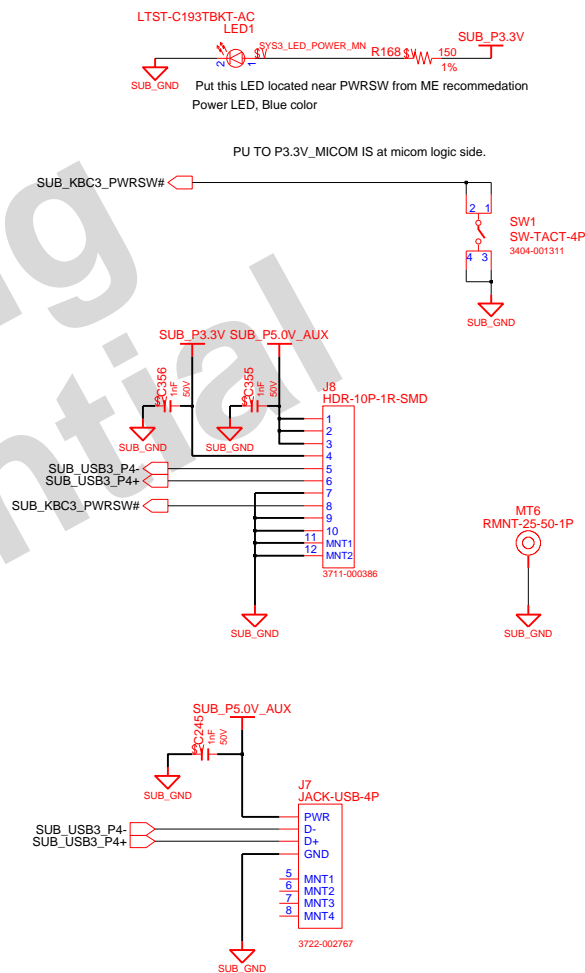
DESIGN	ZHU, JIAN	DATE	6/6/2008	TITLE	Suzhou2-LA USB_DEVICES BLUETOOTH	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01190/
CHECK	GUO, LEI	DEV. STEP	PV			
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 8:13:40 PM	PAGE	44 OF 56	

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**1 PORT USB CONNECTOR**

Adopt P5.0V\_AUX when enable chargeable USB.

**1\*2 PORT USB CONNECTOR****Sub board****Power Switch Button**

DESIGN	ZHU, JIAN	DATE	6/6/2008	TITLE	Suzhou2-LA USB_CONNECTOR USB	<b>SAMSUNG</b> ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV			PART NO. BA41-01190/
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 8:14:54 PM	PAGE	45	OF 56

The schematic diagram illustrates the PWR\_MV\_CHARGER circuit, which manages power from a USB source to charge a battery. Key components and their functions include:

- Power Input:** JACK-DC-POWER-3P-MNT (J1) provides the input power, connected to GND\_1 and GND\_2.
- Power Regulation:** The circuit uses a series of regulators and capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100) to regulate the voltage and current.
- Charging Control:** The circuit includes a charging controller (U1: ISL6254HRZ-T) and a battery management IC (U2: BQ2000) to manage the charging process.
- Battery Interface:** The battery is connected to the circuit via BATT-CONN-7P (J2), which includes pins for BAT3\_DETECT#, BAT3\_SMDATA#, BAT3\_SMCLK#, and BAT3\_BATDET#.
- Protection:** The circuit includes protection diodes (D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, D32, D33, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, D49, D50, D51, D52, D53, D54, D55, D56, D57, D58, D59, D60, D61, D62, D63, D64, D65, D66, D67, D68, D69, D70, D71, D72, D73, D74, D75, D76, D77, D78, D79, D80, D81, D82, D83, D84, D85, D86, D87, D88, D89, D90, D91, D92, D93, D94, D95, D96, D97, D98, D99, D100) and a fuse (F1) to protect the circuit.

The schematic also includes a table for the Adapter configuration:

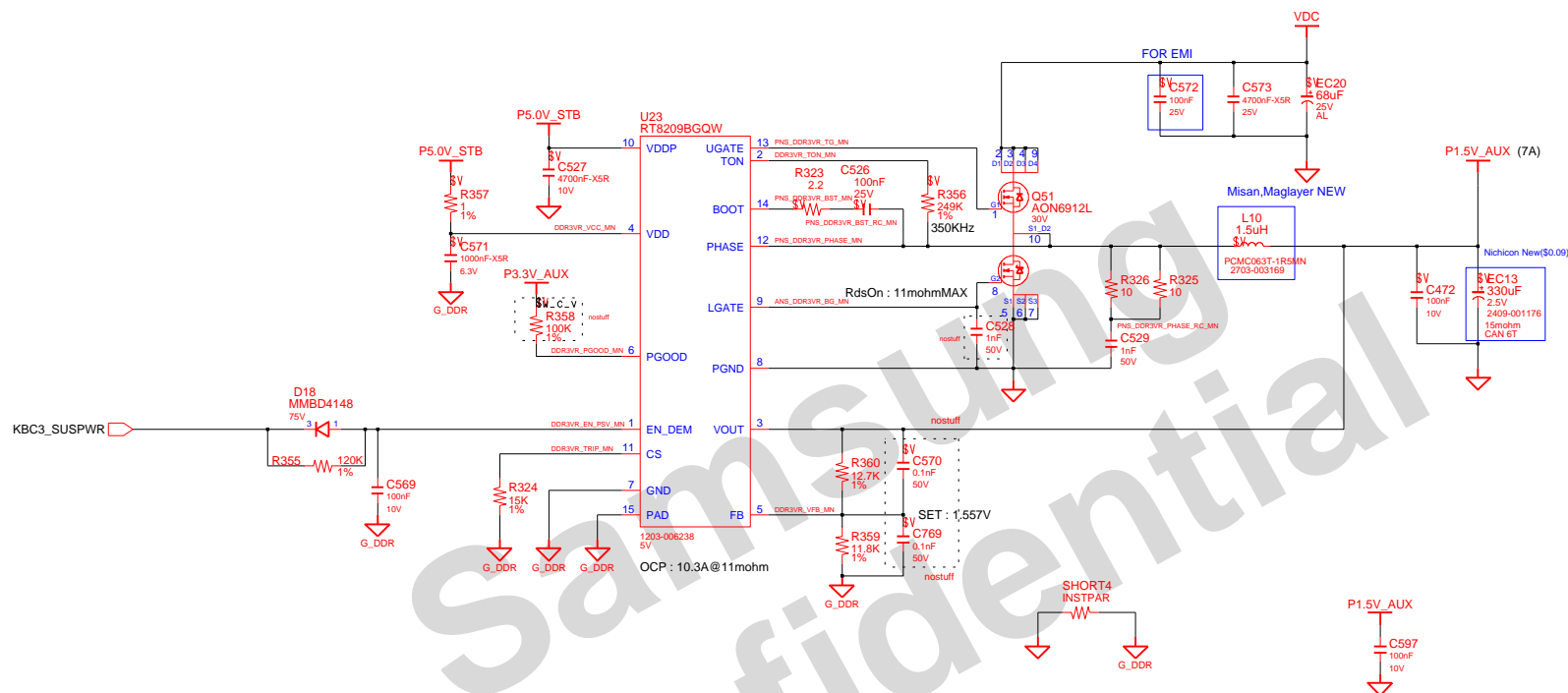
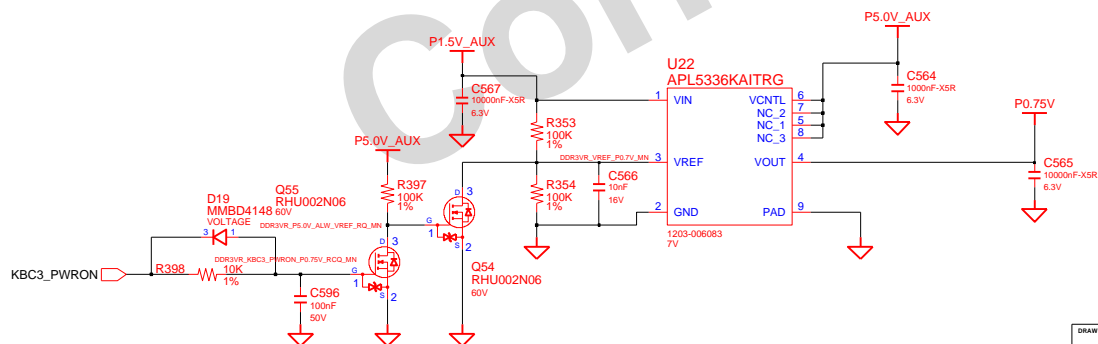
Adapter configuration			
60W / 3.03A / 96%		90W / 4.32A / 91.2%	
Value	SEC Code	Value	SEC Code
Rtop	200K	2007-007334	2007-007142
Rbot	27.4K	2007-007274	2007-008275

The schematic is a detailed representation of the PWR\_MV\_CHARGER circuit, showing the internal components and their connections. It is a complex circuit that requires careful attention to detail for proper assembly and operation.



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**DDR3 Power****DDR3 VTT(0.75V)**

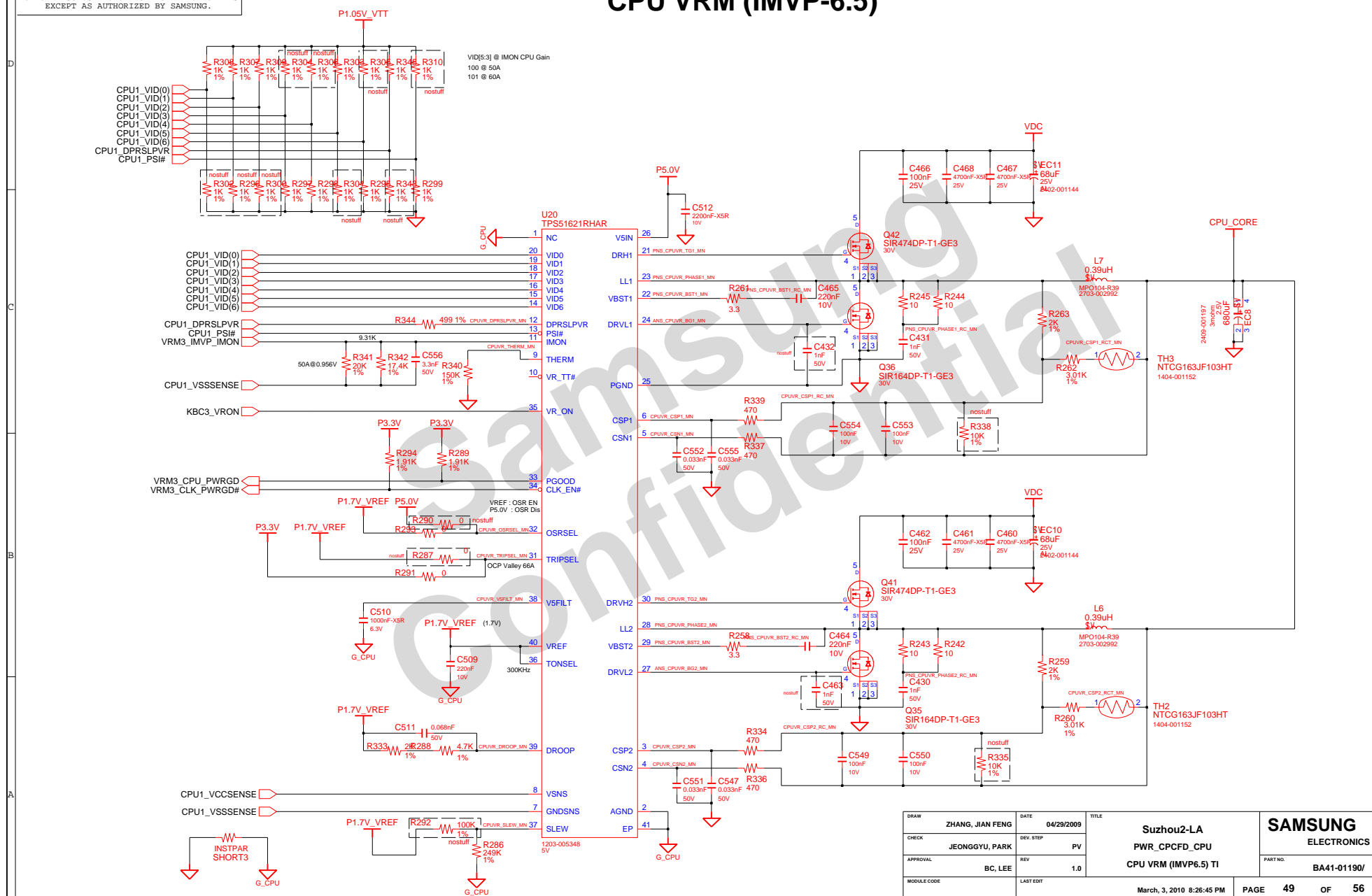
DRAW	ZHANG, JIAN FENG	DATE	03/13/2009	TITLE	Suzhou2-LA	SAMSUNG ELECTRONICS
CHECK	JEONGGYU, PARK	DEV. STEP	PV		PWR_MV_MEMORY	
APPROVAL	BC, LEE	REV	1.0		DDR3 POWER (P1.5V_AUX)	PART NO.
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 8:19:43 PM	PAGE	48	BA41-01190/
				OF	56	



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## CPU VRM (IMVP-6.5)



DRAW	ZHANG, JIAN FENG	DATE	04/29/2009	TITLE	Suzhou2-LA	SAMSUNG ELECTRONICS
CHECK	JEONGGYU, PARK	DEV. STEP	PV		PWR_CPCFD_CPU	
APPROVAL	BC, LEE	REV	1.0		CPU VRM (IMVP6.5) TI	
MODULE CODE		LAST EDIT				
March, 3, 2010 8:26:45 PM						PAGE 49 OF 56

The schematic diagram illustrates the power management section of the RT8209BGQW, showing the internal structure of the RT8209BGQW and the external components connected to its pins. The diagram includes a large watermark "Copyrighted material".

**Internal Structure of RT8209BGQW:**

- Pin 10 (VDDP):** Connected to P5.0V through R9 (5V, 1%) and C18 (4700nF-XSR, 10V).
- Pin 11 (VDD):** Connected to P5.0V through R9 (5V, 1%) and C17 (1000nF-XSR, 6.3V).
- Pin 12 (PGOOD):** Connected to P3.3V through R7 (5V, 1%) and C16 (2200nF-XSR, 10V).
- Pin 13 (UGATE TON):** Connected to P5.0V through R34 (2.2) and C29 (100nF).
- Pin 14 (BOOT):** Connected to P5.0V through R32 (300K, 1%) and C29 (100nF).
- Pin 15 (PHASE):** Connected to P5.0V through R32 (300K, 1%) and C29 (100nF).
- Pin 16 (LGATE):** Connected to P5.0V through R32 (300K, 1%) and C29 (100nF).
- Pin 17 (PGND):** Connected to P5.0V through R32 (300K, 1%) and C29 (100nF).
- Pin 18 (EN\_DEM):** Connected to P5.0V through R32 (300K, 1%) and C29 (100nF).
- Pin 19 (CS):** Connected to P5.0V through R32 (300K, 1%) and C29 (100nF).
- Pin 20 (PAD):** Connected to P5.0V through R32 (300K, 1%) and C29 (100nF).
- Pin 21 (GND):** Connected to P5.0V through R32 (300K, 1%) and C29 (100nF).
- Pin 22 (FB):** Connected to P5.0V through R32 (300K, 1%) and C29 (100nF).

**External Components:**

- Q13:** SIR474DP-T1-GE3, 30V MOSFET.
- Q7:** SIR460DP-T1-GE3, 30V MOSFET.
- Q19:** 1nF, 50V capacitor.
- Q20:** 1nF, 50V capacitor.
- Q21:** 1nF, 50V capacitor.
- Q22:** 1nF, 50V capacitor.
- Q23:** 1nF, 50V capacitor.
- Q24:** 1nF, 50V capacitor.
- Q25:** 1nF, 50V capacitor.
- Q26:** 1nF, 50V capacitor.
- Q27:** 1nF, 50V capacitor.
- Q28:** 1nF, 50V capacitor.
- Q29:** 1nF, 50V capacitor.
- Q30:** 1nF, 50V capacitor.
- Q31:** 1nF, 50V capacitor.
- Q32:** 1nF, 50V capacitor.
- Q33:** 1nF, 50V capacitor.
- Q34:** 1nF, 50V capacitor.
- Q35:** 1nF, 50V capacitor.
- Q36:** 1nF, 50V capacitor.
- Q37:** 1nF, 50V capacitor.
- Q38:** 1nF, 50V capacitor.
- Q39:** 1nF, 50V capacitor.
- Q40:** 1nF, 50V capacitor.
- Q41:** 1nF, 50V capacitor.
- Q42:** 1nF, 50V capacitor.
- Q43:** 1nF, 50V capacitor.
- Q44:** 1nF, 50V capacitor.
- Q45:** 1nF, 50V capacitor.
- Q46:** 1nF, 50V capacitor.
- Q47:** 1nF, 50V capacitor.
- Q48:** 1nF, 50V capacitor.
- Q49:** 1nF, 50V capacitor.
- Q50:** 1nF, 50V capacitor.
- Q51:** 1nF, 50V capacitor.
- Q52:** 1nF, 50V capacitor.
- Q53:** 1nF, 50V capacitor.
- Q54:** 1nF, 50V capacitor.
- Q55:** 1nF, 50V capacitor.
- Q56:** 1nF, 50V capacitor.
- Q57:** 1nF, 50V capacitor.
- Q58:** 1nF, 50V capacitor.
- Q59:** 1nF, 50V capacitor.
- Q60:** 1nF, 50V capacitor.
- Q61:** 1nF, 50V capacitor.
- Q62:** 1nF, 50V capacitor.
- Q63:** 1nF, 50V capacitor.
- Q64:** 1nF, 50V capacitor.
- Q65:** 1nF, 50V capacitor.
- Q66:** 1nF, 50V capacitor.
- Q67:** 1nF, 50V capacitor.
- Q68:** 1nF, 50V capacitor.
- Q69:** 1nF, 50V capacitor.
- Q70:** 1nF, 50V capacitor.
- Q71:** 1nF, 50V capacitor.
- Q72:** 1nF, 50V capacitor.
- Q73:** 1nF, 50V capacitor.
- Q74:** 1nF, 50V capacitor.
- Q75:** 1nF, 50V capacitor.
- Q76:** 1nF, 50V capacitor.
- Q77:** 1nF, 50V capacitor.
- Q78:** 1nF, 50V capacitor.
- Q79:** 1nF, 50V capacitor.
- Q80:** 1nF, 50V capacitor.
- Q81:** 1nF, 50V capacitor.
- Q82:** 1nF, 50V capacitor.
- Q83:** 1nF, 50V capacitor.
- Q84:** 1nF, 50V capacitor.
- Q85:** 1nF, 50V capacitor.
- Q86:** 1nF, 50V capacitor.
- Q87:** 1nF, 50V capacitor.
- Q88:** 1nF, 50V capacitor.
- Q89:** 1nF, 50V capacitor.
- Q90:** 1nF, 50V capacitor.
- Q91:** 1nF, 50V capacitor.
- Q92:** 1nF, 50V capacitor.
- Q93:** 1nF, 50V capacitor.
- Q94:** 1nF, 50V capacitor.
- Q95:** 1nF, 50V capacitor.
- Q96:** 1nF, 50V capacitor.
- Q97:** 1nF, 50V capacitor.
- Q98:** 1nF, 50V capacitor.
- Q99:** 1nF, 50V capacitor.
- Q100:** 1nF, 50V capacitor.

**Other Components:**

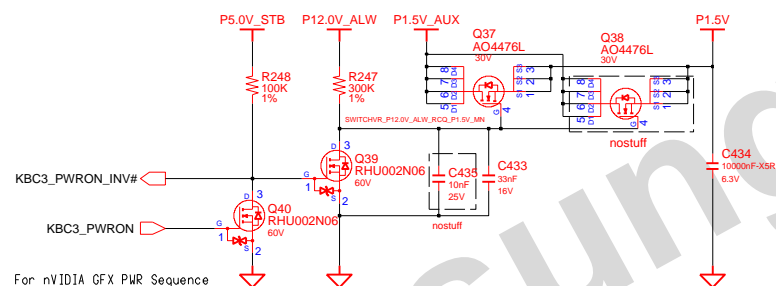
- C46:** 100nF, 25V capacitor.
- C48:** 4700nF-XSR, 25V capacitor.
- C50:** 4700nF-XSR, 25V capacitor.
- EC2:** 68uF, 25V AL electrolytic capacitor.
- C47:** 100nF, 10V capacitor.
- EC5:** 330uF, 2.5V electrolytic capacitor.
- EC1:** 330uF, 2.5V electrolytic capacitor.
- C28:** 47nF, 50V capacitor.
- R11:** 10K, 1% resistor.
- R33:** 22K, 1% resistor.
- R8:** 6.19K, 1% resistor.
- R10:** 15K, 1% resistor.
- R35:** 10, 1% resistor.
- R36:** 10, 1% resistor.
- R37:** 10, 1% resistor.
- R38:** 10, 1% resistor.
- R39:** 10, 1% resistor.
- R40:** 10, 1% resistor.
- R41:** 10, 1% resistor.
- R42:** 10, 1% resistor.
- R43:** 10, 1% resistor.
- R44:** 10, 1% resistor.
- R45:** 10, 1% resistor.
- R46:** 10, 1% resistor.
- R47:** 10, 1% resistor.
- R48:** 10, 1% resistor.
- R49:** 10, 1% resistor.
- R50:** 10, 1% resistor.
- R51:** 10, 1% resistor.
- R52:** 10, 1% resistor.
- R53:** 10, 1% resistor.
- R54:** 10, 1% resistor.
- R55:** 10, 1% resistor.
- R56:** 10, 1% resistor.
- R57:** 10, 1% resistor.
- R58:** 10, 1% resistor.
- R59:** 10, 1% resistor.
- R60:** 10, 1% resistor.
- R61:** 10, 1% resistor.
- R62:** 10, 1% resistor.
- R63:** 10, 1% resistor.
- R64:** 10, 1% resistor.
- R65:** 10, 1% resistor.
- R66:** 10, 1% resistor.
- R67:** 10, 1% resistor.
- R68:** 10, 1% resistor.
- R69:** 10, 1% resistor.
- R70:** 10, 1% resistor.
- R71:** 10, 1% resistor.
- R72:** 10, 1% resistor.
- R73:** 10, 1% resistor.
- R74:** 10, 1% resistor.
- R75:** 10, 1% resistor.
- R76:** 10, 1% resistor.
- R77:** 10, 1% resistor.
- R78:** 10, 1% resistor.
- R79:**

DRAW	ZHANG, JIAN FENG	DATE	03/11/2009	Suzhou2-LA		<b>SAMSUNG</b> ELECTRONICS	
CHECK	JEONGGYU, PARK	DEV. STEP	PV				
APPROVAL	BC, LEE	REV	1.0	CHIPSET POWER(P1.05V_VTT,P1.5V)		PART NO.	BA41-01190/
MODULE CODE		LAST EDIT		March, 3, 2010 8:25:57 PM		PAGE	50 OF 56



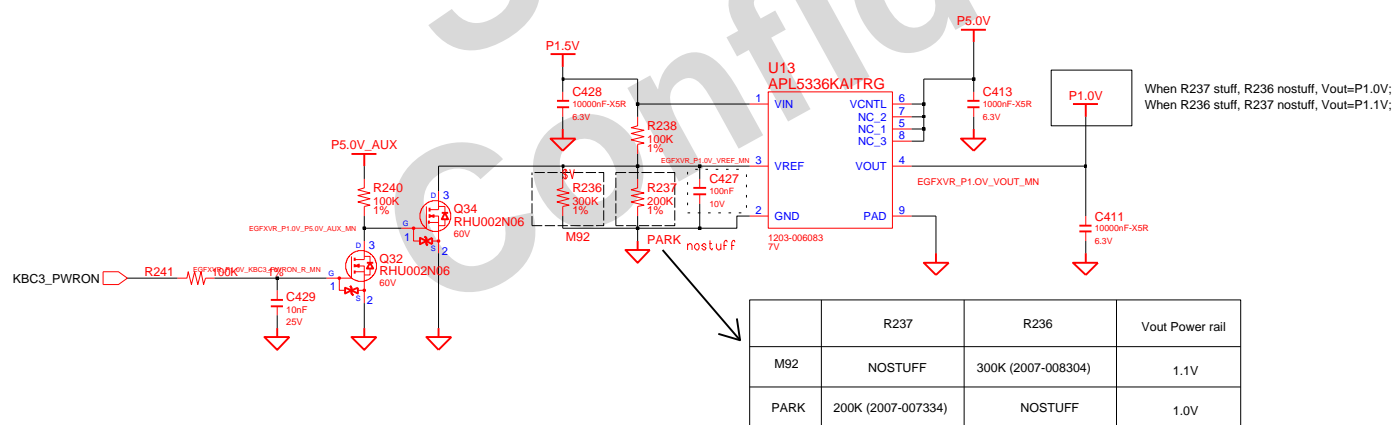
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**gDDR3 POWER(P1.5V)**

For nVIDIA GFX PWR Sequence

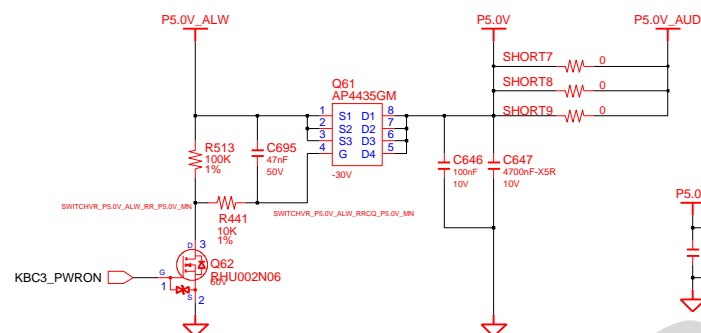
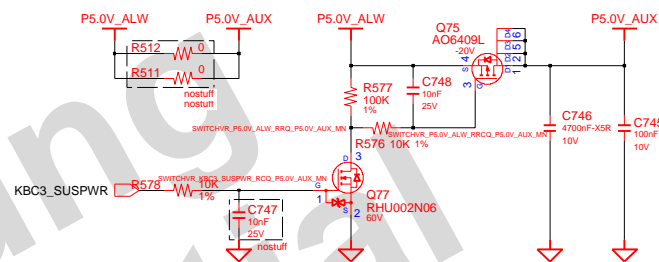
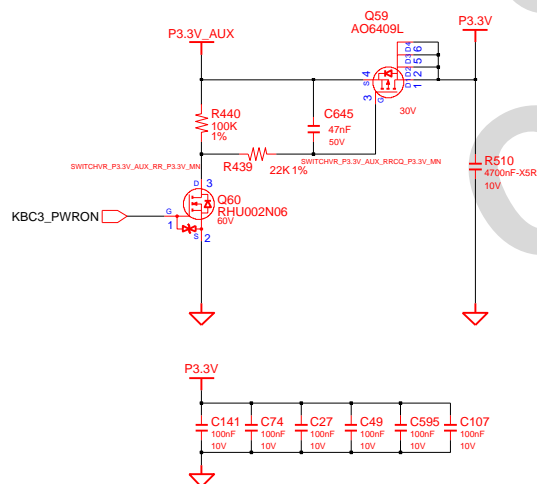
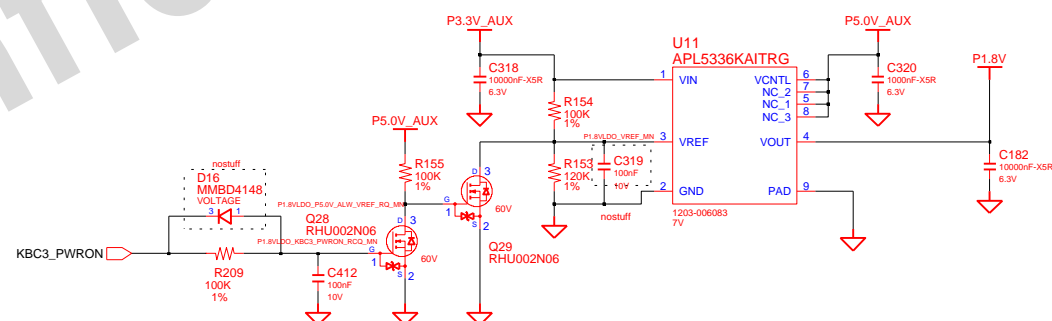
NVDD(EGFX\_CORE) first and then FBVDDQ(gDDR3)

**P1.0V/P1.1V**

DRAW	ZHANG, JIAN FENG	DATE	08/18/2009	TITLE	Suzhou2-LA	SAMSUNG
CHECK	JEONGGYU, PARK	DEV. STEP	PV		PWR_GFX MEMORY	ELECTRONICS
APPROVAL	BC, LEE	REV	1.0		gDDR3 POWER	PART NO.
MODULE CODE		LAST EDIT	March, 3, 2010 8:28:15 PM	PAGE	52	BA41-xxxxxx
				OF	56	

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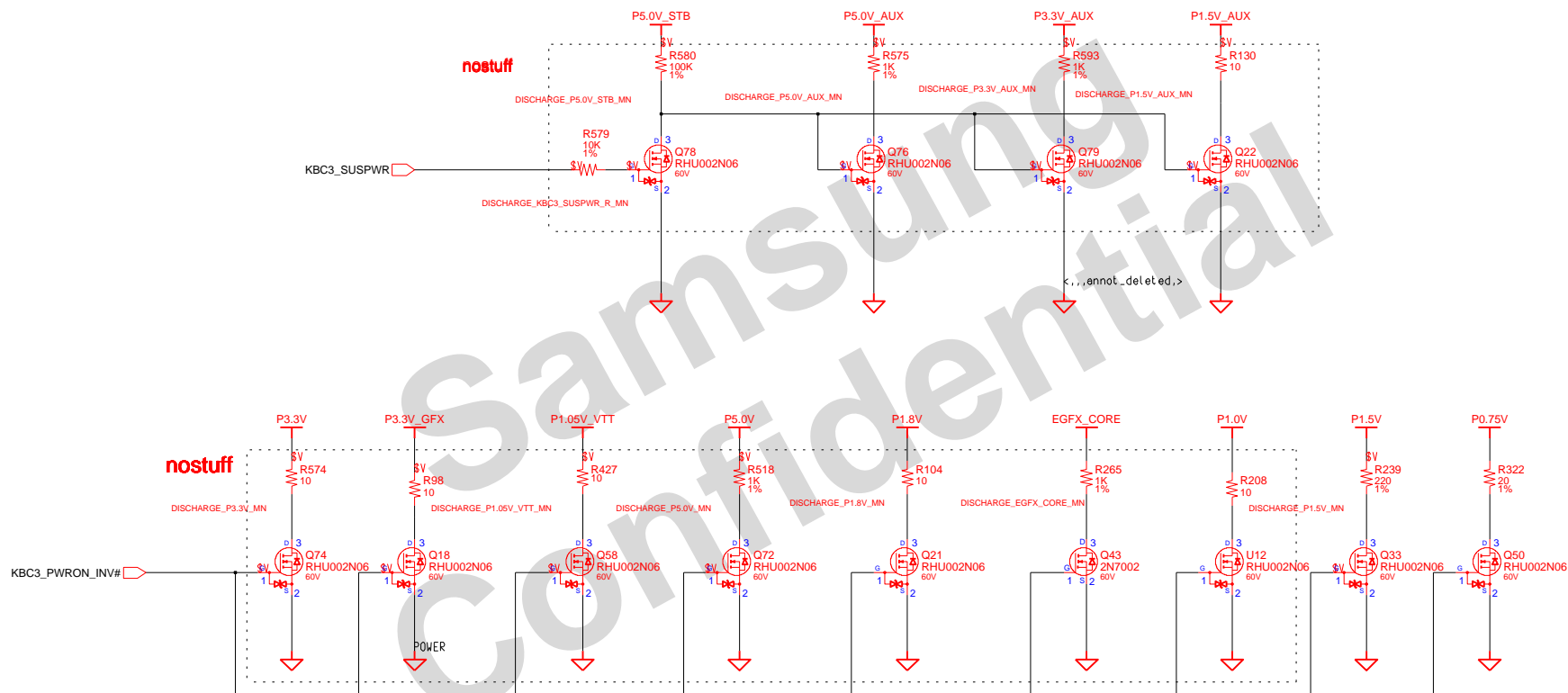
**SWITCHED POWER****Switched Power On (P5.0V)****Sleep'n Charger****Switched Power On (P3.3V)****P1.8V(LDO)**

DRAW	ZHANG, JIAN FENG	DATE	03/11/2009	TITLE	Suzhou2-LA	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01190/
CHECK	JEONGGYU, PARK	DEV. STEP	PV		PWR_MV_SWITCHED	
APPROVAL	BC, LEE	REV	1.0		SWITCHED POWER	
MODULE CODE	undefined	LAST EDIT	March, 3, 2010 8:30:19 PM	PAGE	53 OF 56	

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# POWER DISCHARGER

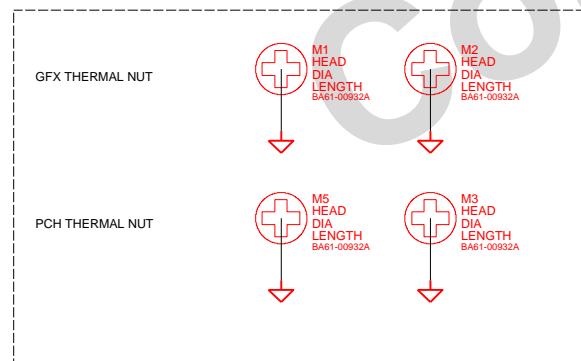
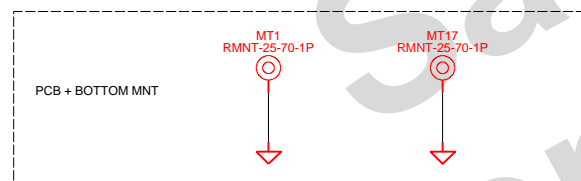
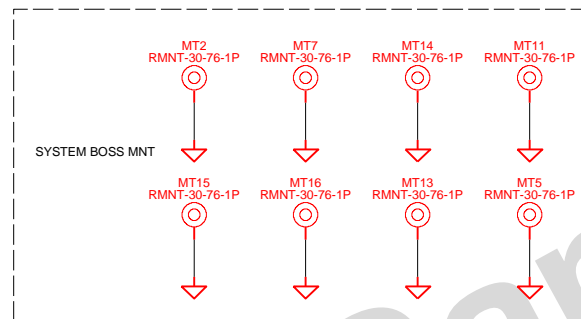
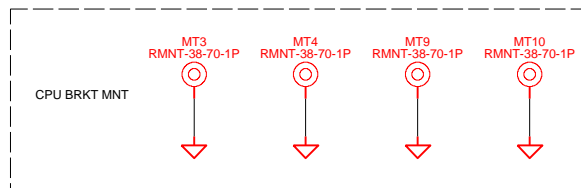


DESIGN	ZHANG, JIAN FENG	DATE	3/3/2010	TITLE	Suzhou2-LA PWR_MV_DISCHARGER	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01190/
CHECK	JEONGGYU, PARK	DEV. STEP	PV			
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE		LAST EDIT	March, 3, 2010 8:34:57 PM	PAGE	54 OF 56	

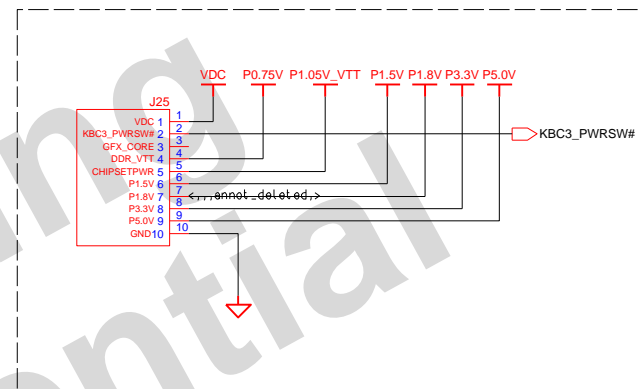
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# MOUNT HOLE



## ICT PORT



DRAW	ZHU, JIAN	DATE	03/11/2009	TITLE	Suzhou2-LA MAIN MOUNT HOLE	SAMSUNG ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV			PART NO. BA41-01190/
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE		LAST EDIT	March, 3, 2010 8:38:12 PM	PAGE	55	OF 56

